Adaptive Sensitivity™ CCD Image Sensor

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ABSTRACT

The design of Adaptive Sensitivity CCD Image Sensor is described. The sensitivity of each pixel is individually controlled (by changing its exposure time) to assure that it is operating in the linear range of the CCD response, and not in the Cut-off or Saturation regions. Thus, even though an individual CCD sensor is limited in its dynamic range, the whole CCD array has a much wider dynamic range. The idea is based on the biological retina principle of operation, enabling the imager to capture details in both the light and dark areas of high-contrast scenes, as in the human eye.

1. INTRODUCTION

CCD image sensors are relatively limited in their dynamic range to about 1000:1 at normal temperatures (10 bits, or 60 dB). At the same time, the luminance of natural and man-made scenes often spans a dynamic range 10-100 times as much. Thus, normal electronic acquisition is quite limited, in the sense that one image either captures the highlights of the scene or the shadows, but not both. The (simplified) response of a typical CCD image sensor is shown in Figure 1.

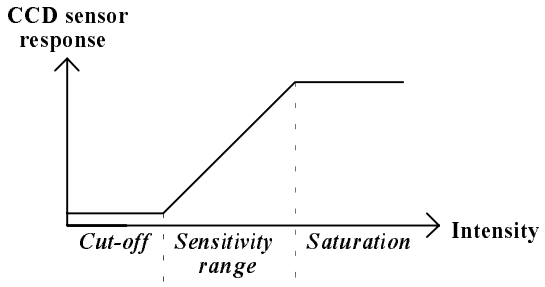

Figure 1: The response of a CCD sensor

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Due to the limited dynamic range of the sensor, normal electronic acquisition is often characterized by images having some cut-off pixels and some saturated pixels, in addition to valid image pixels.

One solution to the problem of limited dynamic range is based on logarithmic sensors. The "PhotoFET" [1] logarithmically acquires up to 4.5 orders of magnitude intensity levels. Mead [2] described the Silicon Retina, which not only employs bipolar phototransistors as logarithmic sensors, but also utilizes a computational analog network at the focal plane to enhance the image data according to a mechanism resembling that of the human eye.

The motivation for the Silicon Retina is based on the observation that the dynamic range of the human retina is much wider than that of electronic sensors, reaching as high as $1{:}10^8$. This superb performance is attributed to the fact that each receptor of the retina is individually adjustable, so that receptors which receive high levels of luminance turn their sensitivity down, while receptors staring at the darker parts of the scene increase their gain. Thus, while each individual receptor may still be limited in its basic dynamic range, the whole retina is capable of acquiring images having extremely wide dynamic range. The *Adaptive Sensitivity (A/S)* CCD imagers described in this paper operate according to exactly the same principle.

In the rest of this paper we describe some alternative architectures for the sensor and their operation, the controlling algorithms, and the global system architecture.

2. SENSOR ARCHITECTURE

Variable exposure time is used as the main tool for controlling pixel sensitivity. The charge which accumulates in a CCD cell is proportional to the exposure time and is given [3] by

$$Q = c\,I\,T$$

where I is the incident irradiance, T is the exposure time, and c is a constant (depending upon the sensor responsivity and its area). Controlling the exposure time of individual cells in the CCD array is designed to assure that each cell is operating in the linear range of their response. Thus, pixels receiving low light intensity are exposed for longer time, and pixels receiving high intensity levels are exposed for shorter time, preventing them from getting saturated. In this way, the dynamic range of the entire CCD array is expanded. As a side benefit of this scheme, note that since no pixel is allowed to get saturated, blooming (namely, the spill-off of charges from a saturated pixel to neighboring ones) is also eliminated. Thus, the A/S CCD is also inherently an anti-blooming sensor.

The A/S sensor architecture shown in Figure 2 extends the common interline-transfer design with registers and logic for controlling the sensitivity of the individual pixels of the array.

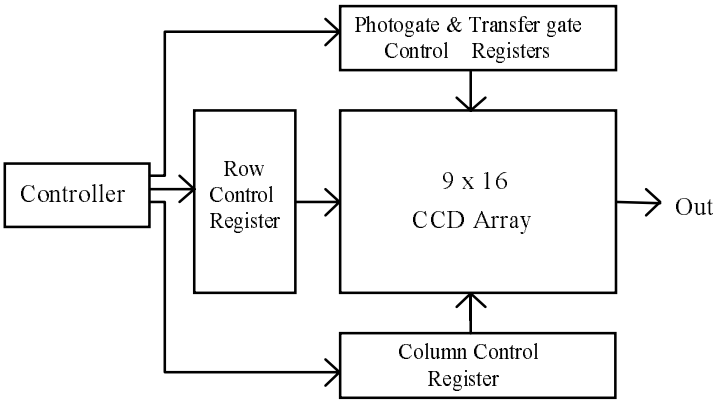

Figure 2: The A/S CCD Imager Chip Architecture

One possible design of the individually controlled CCD sensor cell, as shown in Figure 3, consists of an N+ diffusion area connected to Vdd, a Reset gate, a photosensitive MOS capacitor under a Photogate, a Transfer gate and a segment of the vertical interline CCD shift register.

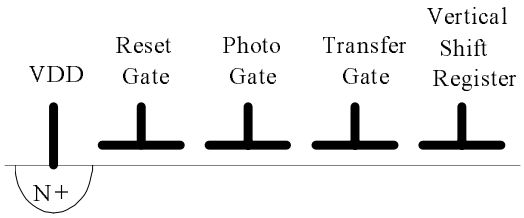

Figure 3: CCD Sensor Cell Structure

Controlling the exposure time of the CCD cell is achieved by activating the Reset gate, thereby discharging the photosensitive capacitor. The integration period is common and simultaneous to the whole array, but for each individual pixel that period is divided into two parts: Discharge and Integrate. The higher the level of incident illumination, the shorter the Integrate part should be. During the Discharge part, when accumulation of charges under the Photogate is to be avoided, the Reset gate is kept at high voltage, and the collected photo-charges are spilled off to the diffusion area, which can be considered an infinitely deep potential well. For accumulation, the Reset gate is turned low and charges are collected in the potential well under the Photogate. Once the integration period is over, charge packets are transferred as usual in interline CCDs.

Two alternative architectures are employed for controlling the Reset gate. In the register-based architecture, the Reset gate is controlled by a Set-Reset Flip-Flop (see Figure 4). The FF's Set line is global to the whole array. The FF's Reset line is separately connected to each cell, and is derived by the logical AND of the appropriate Row and Column control lines for the specific cell.

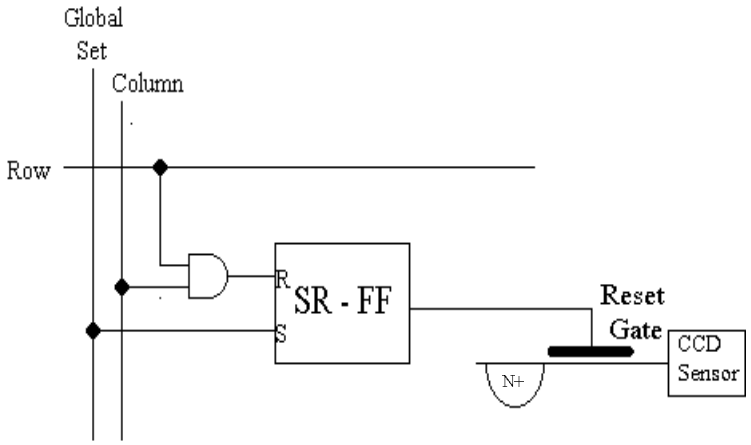

Figure 4: Reset Gate Control

The alternative architecture employs two Reset gates in sequence, instead of one, and connects the Row and Column wires directly to the two Reset gates respectively. While alleviating the need for a FF-per-pixel, and thus substantially increasing the fill factor, that architecture requires that multiple reset pulses are applied repeatedly to each pixel throughout its Discharge period, thus possibly generating a certain level of switching noise. Most of our experimental research is focused on the FF-per-pixel architecture, due its more robust and static nature, but we believe that ultimately the latter, dynamic architecture will prove more efficient.

3. IMAGING CHIP ARCHITECTURE AND OPERATION

The FF-per-pixel A/S sensor operates as follows. Each video frame is allocated an integration period of fixed length. Each individual pixel can be exposed for any time period less than, or equal to, the maximum full frame integration time. In the beginning of the frame time all the control FFs are globally set, so that no charge can accumulate. During the frame integration time, the control circuit, in response to control signals received from an external controller, resets individual FFs, enabling charge accumulation in the respective cells. At the end of the frame integration time, all charges are transferred to the interline registers, and then out of the sensor chip.

Control of resetting the FFs is executed serially in columns. The *column control register* (Figure 2) contains a shift register with a single '1' circling around. When the '1' bit is at column *i*, the *row control register* receives a column of ones and zeroes, where a one corresponds to a FF in column *i* which must be reset. Those FFs for which both row and column lines are '1' are reset, and as a result charges start accumulating in those cells.

This process is repeated for each different exposure time. Note that, since the process progresses sequentially over the columns of the array, integration starts occur in a staggered order. This effect is compensated for during charge read-out, as explained below.

While this scheme of operation allows very accurate control of the exposure time of each pixel, in our experimental chips we contend with a choice of just three different exposure time intervals, which suffice to produce, for example, 14 bit wide dynamic range signal. Suppose each exposure spans an 8 bit dynamic range, and that the ratio of the three exposure times is 1:8:64. Then the first exposure time can generate pixel values in the relative range of 1 through 256, the second exposure time can generate values in the range 8 through 2048 (at increments of 8 levels), and the third exposure time can generate values in the range 64 through 16384 (at increments of 64 levels), thus covering a total range of $1:2^{14}$.

Once the frame integration time is over, charges are transferred from the sensor area to the CCD shift register, and subsequently outside of the chip. To compensate for the staggered starting of all integrations, read-out is also staggered by columns. To achieve this, the Photogates and Transfer gates are enabled one column after another, using the *Photogate & Transfer gate control registers* (Figure 2) with a single '1' bit circling around each shift register.

4. SYSTEM ARCHITECTURE AND OPERATION

The global system architecture is shown in Figure 5. The external controller receives the CCD output directly from the A/S CCD sensor. For each pixel, the corresponding exposure time is retrieved from the controller's *exposure time memory*. If the pixel value is out of bounds (saturated, or too low), the corresponding exposure time is modified, if possible, by the *update controller* and stored back in memory. The image data and the exposure time used to acquire it are also passed on to an *image processor* for computing of the output image.

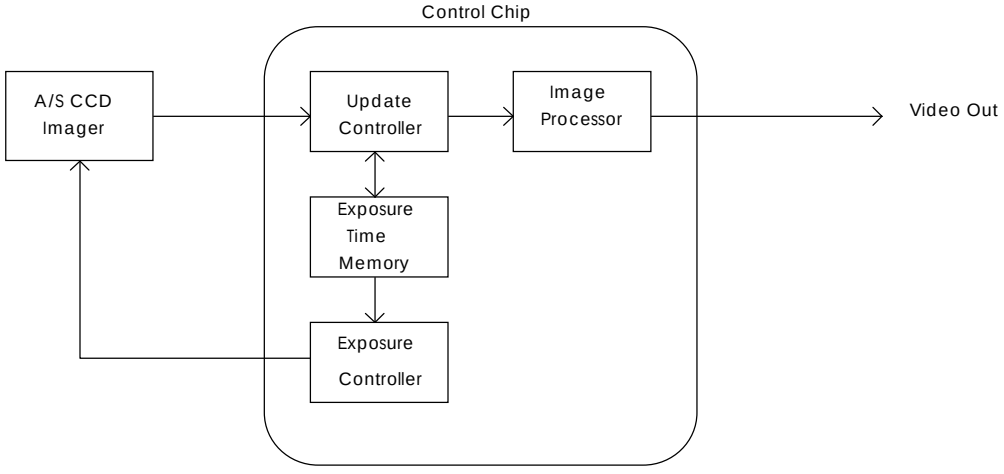

Figure 5: System Architecture

The image processor can compute the output image according to any one of a number of alternative algorithms. One such algorithm [4] is based on first computing a wide dynamic range image data from

the pixel values and their relative exposure times, as explained above, followed by combining a pseudo-logarithmic transform of the wide dynamic range pixel value with spatially-localized edge enhancement.

In parallel, and independently, the *exposure controller* scans the exposure time memory, and sends control signals to the CCD imager that are used for resetting the various FFs, as described above.

Note that the update process described above assumes stationary levels of light intensity between frames, since the newly computed exposure time does not take effect before the next frame. When there are changes in the luminance data (due to lighting change, or due to movement), convergence is usually achieved within one frame time, and after two frames at the most (when there are only three possible exposure times).

5. TEST CHIP DESIGN AND TEST

The layout of a tiny 2.2x2.2 mm^2 9×16 experimental A/S CCD imager test chip [5] is shown in Figure 6. Electrical and electro-optical tests were performed. The video output signal is 3V at saturation of about 320,000 electrons. The CCD output is linear in both exposure time and illumination. Presently we are also experimenting with CMOS sensors, alleviating the need to resort to special processes for CCD.

Figure 6: A/S CCD Imager Test Chip Layout

6. SUMMARY

The A/S CCD image sensor allows individual adjustment of the sensitivity of each pixel, independent of the other pixels. As a result, the sensor can acquire a much wider dynamic range image data than is usually possible with electronic image sensors.

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