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A Low–Power Spike Detection and Alignment Algorithm

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***Abstract*–Front-end integrated circuits for signal processing are useful in neuronal recording systems that engage a large number of electrodes. Detecting, alignment, and sorting the spike data at the front-end reduces the data bandwidth and enables wireless communication. Without such data reduction, large data volumes need to be transferred to a host computer and typically heavy cables are required which constrain the patient or test animal. Front-end processing circuits can dissipate only a limited amount of power, due to supply constraints and heat restrictions. Reduced complexity spike detection and alignment algorithm and architecture, based on Integral Transform, are introduced. They achieve 99% of the precision of a PCA detector, while requiring only 0.05% of the computational complexity.**

I. INTRODUCTION

Automatic and semiautomatic approaches to the reconstruction and analysis of neuronal activity have been the subject of extensive research [1][2]. Typical settings of neuronal recording experiments in test animals and human subjects require high bandwidth communications from the recording electrodes to the processing computer, where spikes are detected and sorted. When a large number of recording electrodes is needed, typical transmission resources are insufficient and power-hungry [3]. In addition, the large number of wires results in heavy cables that severely constrain the subject. Consequently, it is desirable to pre-process and reduce the volume of the recorded data so that it can be transmitted wirelessly.

We investigate implantable integrated circuits for power-efficient front-end processing of spikes, in order to minimize the communication bandwidth from the recording electrodes to the back-end computer [4]. In this paper we focus on power-efficient *detection and alignment* (D&A) of spikes as a pre-requisite to successful on-chip spike sorting [5]. For instance, given a sampling rate of 24Ksps and 12 bit sampling precision, the raw data rate is 288Kbits/second. Spike D&A enables transmission of only active spike data and filtering out the inter-spike noise [6]. Assuming a high rate of 100 spikes/sec/electrode and 2msec/spike, D&A reduces the data rate to 60Kbits/sec. Spike sorting converts each spike to a short datagram (~20 bits), reducing the required data rate down to 2Kbits/sec per electrode, less than 1% of the original rate.

Power requirements of typical D&A algorithms could be prohibitively high for simultaneous recording form a large number of electrodes. We consider D&A algorithms and architectures that trade off some subsequent classification accuracy in return for significant savings in power. A similar approach has been presented in [7]. Spike detection algorithms have also been discussed in [3][8]-[12].

We introduce the *Maximum Integral Transform Alignment* (MITA) algorithm for spike D&A, and compare it with an algorithm based on principal components analysis (MPA). The MITA algorithm achieves 99% classification accuracy for about 0.05% of the computational efforts of PCA spike D&A. The system is overviewed in Section II. The algorithms and architectures are described in Section III, and their performance is analyzed in Section IV.

II. SYSTEM OVERVIEW

In typical experimental setups, the signals recorded by the electrodes are amplified and transmitted over wires to a host computer where they are digitized and processed according to the experimental requirements [13]. The main disadvantage of that experimental arrangement is the need to connect a cable to the subject, restricting its movement. The Neuroprocessor (an implantable integrated circuit) performs front-end analog processing, spike D&A and spike sorting, achieving significant data reduction and thus enabling wireless communications that replace cables and allow free movement of the patient or test subject.

The architecture of the part of the Neuroprocessor that processes the signal from a single electrode is shown in Figure 1. Spike processing must be adaptable, due to unstable recording conditions [3][10]. Therefore, periodically, raw data is transmitted to the host computer for training, and the recalculated parameters are sent back to the Neuroprocessor. The Spike Detector detects the presence of spikes in the input, determines their starting point, and initiates the operation of the Spike Sorter. The output logic produces the spike notification datagram.

Performance of the spike sorter depends critically on the accuracy of the D&A algorithm. In this paper we focus on the D&A algorithms and assume a given Spike Sorter.

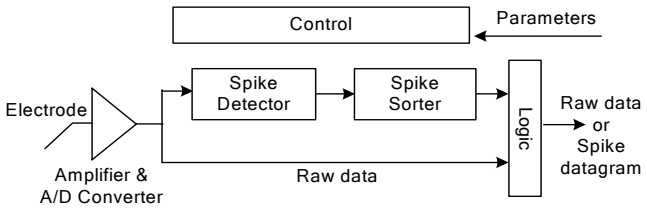

Figure 1: Neuroprocessor Architecture: one electrode section

III. SPIKE DETECTION AND ALIGNMENT: ALGORITHMS AND ARCHITECTURES

When exploring algorithms and VLSI architectures for real time spike D&A to be carried out at the head-stage, we seek to minimize power dissipation while still achieving acceptable levels of sorting accuracy. Following [14], we consider the relative computational complexity of two architectures as a predictor of their power requirements.

A. Maximum Projection Algorithm (MPA)

The *Maximum Projection* algorithm (MPA) is based on the analysis of principal component (PC) metrics. This algorithm is a VLSI-oriented version of a common software detection algorithm [15]. It consists of on-line detection and off-line learning, which determines processing parameters. The PC metrics represent the projections of the input signal on the first two principal component vectors [16]. The MPA algorithm comprises two steps: *extraction* and *alignment*. During extraction, a segment of the continuous input signal is extracted. Extraction is triggered by threshold crossing at the input (threshold level is determined in advance by off-line learning). The segment is digitized into $M=K+N$ samples. The first K samples precede the threshold crossing time, and the remaining N samples follow that time. The alignment step seeks a spike of N samples long within the M samples segment, starting at an offset $i \in \{1,...,K\}$ from the beginning of the segment. Thus, alignment searches for the best offset i, namely the offset that yields the minimum error between the estimated and input signals.

A VLSI architecture for on-chip D&A by means of principal component analysis (PCA) using two principal components is shown in Figure 2. Off-line learning and tracking provides PC and threshold values to the algorithm. The input is transferred through a FIFO register of K stages. The Threshold unit triggers operation of the Estimation unit. The Estimation unit computes the $2K$ projections on the two PC vectors (two projections at each offset i) and produces the estimated signal per each i. Once the Min Error unit finds the offset that yields the minimal estimation error, the corresponding projections $P1_i$ and $P2_i$ are sent to the output. Note that if no minimum is detected within the range of possible offsets, the last offset is selected. The performance of this architecture is described in Section IV below.

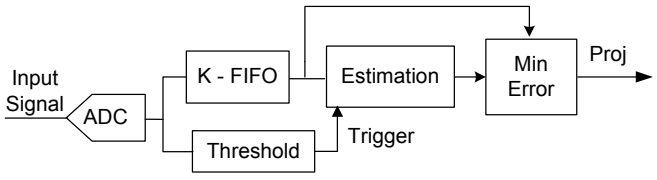

Figure 2: MPA - VLSI architecture

B. Maximum Integral Transform Alignment Algorithm (MITA)

The Maximum Integral Transform Alignment algorithm (MITA) is based on separate integration of the positive and negative phases of the spike. We assume that the spike signal can be split into two time intervals A and B, typically according to the positive and negative phases of the spike (Figure 3). The length of these intervals and their relative position is determined by off-line learning. The MITA algorithm computes two integrals of the signal, over A and B, respectively. As in the MPA case, the MITA algorithm comprises two steps, *extraction* and *alignment*. The extraction step is the same as for MPA. Alignment is determined by finding the maximum of the A integral. Once it has been determined, both A and B integral values are produced at the output and may be employed for subsequent spike sorting.

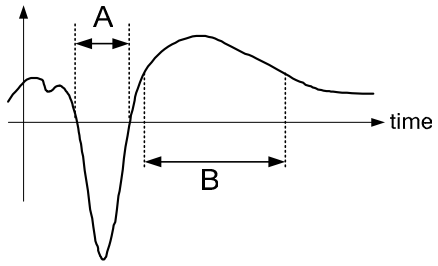

Figure 3: Two integration time intervals A, B for the IT D&A algorithm

A conceptual VLSI architecture for the MITA algorithm is shown in Figure 4. Note that integrals A and B do not overlap in time, and thus we first compute integral A, find the best offset, and only then compute integral B.

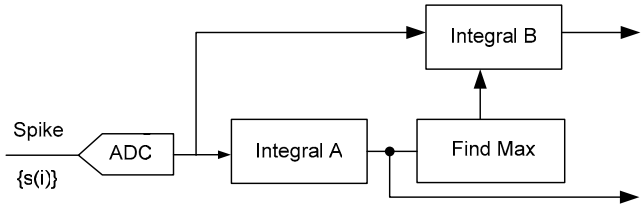

Figure 4: Digital MITA - VLSI architecture

The integration procedure can be considered as the result of passing the input signal through a Moving Average filter. A recursive implementation of the Moving Average filter is depicted in Figure 5. Unlike the MPA architecture, there is no need to maintain K sums in parallel: Consider the A integrals,

$$IA_i = \sum_{r=1}^{DA} s_{r+i} \qquad (1)$$

where DA is the number of samples in the A time interval. Then

$$IA_{i+1} = IA_i + s_{i+DA} - s_i \qquad (2)$$

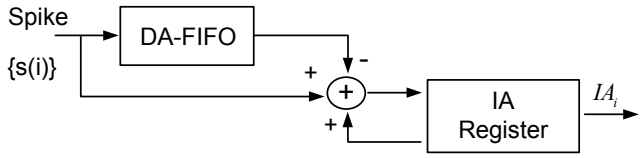

Figure 5: Architecture of the Integral A-unit

Initially, the DA-FIFO contains DA zeros. During the first DA steps, the accumulator computes IA_1. Henceforth, one old element is subtracted from IA and a new one is added.

Thanks to eliminating multiplications, the MITA architecture incurs a significantly lower computation cost than MPA.

IV. RESULTS

A. *Algorithm Validation*

The Neuroprocessor spike D&A algorithms described above are compared (by simulation) to a software implementation of PCA [15][16]. All algorithms are applied to the same data set. Figure 6 illustrates the algorithm validation scheme. First, part of the data is used for off-line training, producing configuration parameters for the algorithm. Second, the parameters are downloaded to the Neuroprocessor simulation model. Third, a simulation of the Neuroprocessor spike D&A algorithm is applied to the entire data set. Once the PCA based software D&A algorithm is also executed on the same data, the results are sorted by a software spike sorting algorithm [17] and then are compared.

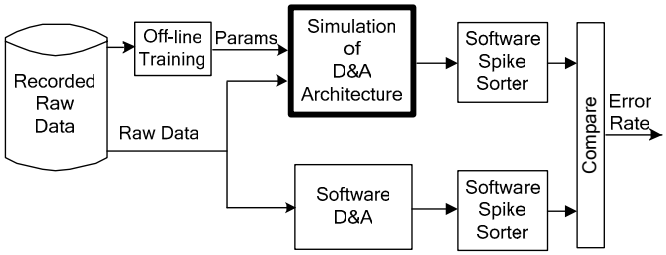

Figure 6: Algorithm validation

Note that we do not compare the results of alignment of the software algorithm vs. those of the Neuroprocessor; rather, we employ spike sorting before making the comparison. This is due to the fact that the sorted results are more meaningful than the raw alignments: Certain variations in spike alignment do not affect spike sorting, so they are filtered out anyway by the sorter.

B. *Spike Data Preparation*

Real spike data was taken from electrophysiological recordings of multiple spike trains, obtained from microelectrodes implanted in multiple cortical regions [17][18]. Neuronal signals from the electrodes were amplified, band-pass filtered (300 – 6000 Hz, four poles Butterworth filter), and sampled at 24 Ksps/electrode. The data is up-sampled 4 times for improved alignment precision. Spikes last about 2 msec, resulting in 200 samples points. Spike detection and alignment were first applied by the software algorithm; only stable spike trains (as judged by stable spike waveforms, stable firing rate and consistent responses to behavioral events) were included in this study. The data set contained about 1,000 spikes per cluster. The projections of recorded spikes on PC space are shown in Figure 7.

C. *Analysis of Spike D&A Algorithms*

The results of a linear classifier applied to the results of the MPA and MITA D&A algorithms are shown in Figure 7 and Figure 8, respectively. The two algorithms are compared in terms of computational complexity and accuracy of D&A, due to the danger that any reduction in computational complexity may come at the expense of precision. We count the number of additions and multiplications required in each case per each spike. Multiplication is counted as about ten additions, and total computational complexity is expressed as the total number of equivalent additions. The computational complexity is roughly proportional to the relative power consumption of each algorithm. The results are shown in Table 1 for K=50 and for spikes 200 samples long. It is evident that (a) the MPA algorithm performs as well as software D&A but incurs a high complexity (and power); (b) the MITA spike sorting algorithm achieves about 99% precision at about 0.05% of the complexity (relative to MPA).

The two spike D&A algorithms were applied to a difficult data set, in which the two spike clusters were very close to each other, and we chose two classification polygons that shared one common edge. The error rate of the two algorithms was maximal in this case; when the clusters are further apart, lower detection and alignment error rates are obtainable.

TABLE 1: COMPUTATIONAL COMPLEXITY AND CLASSIFICATION ERRORS OF THE SPIKE D&A ARCHITECTURES

Algorithm	Add	Mult	Computational Complexity	Error Rate
MPA	50,000	50,000	550,000	0.0%
MITA	250	0	250	1.2%

M=K+N=250, K=50, N=200

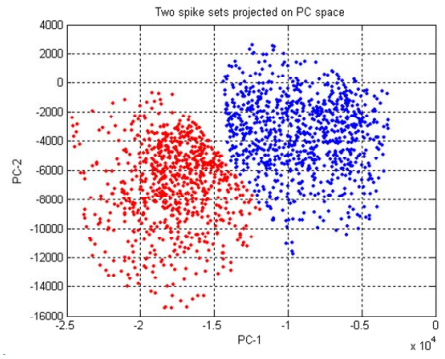

Figure 7: Classification results of the simulated MPA algorithm

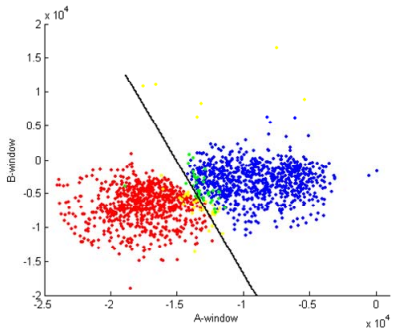

Figure 8: Classification results of the simulated MITA algorithm

V. CONCLUSIONS

We have considered low-power architectures for spike D&A integrated circuits. Such systems may be useful for implanting near recording electrodes, or for using in large multi-electrode arrays, in either research or clinical applications. These systems enable substantial reduction of the communication bandwidth, which is essential when a large number of recording electrodes is involved. We have described two VLSI architectures for spike D&A: MITA integrates the signal in segments and MPA implements a common PCA analysis. The algorithms have been simulated with real data obtained from neuronal recordings. The results are analyzed in terms of classification errors (relative to sorting achieved with software PCA classification) and computational complexity (estimated based on the number of additions and multiplications). The MITA algorithm yields only marginal accuracy degradation relative to MPA, while incurring only a very small fraction of the computational complexity. Thus, we have selected the MITA algorithm for power-efficient spike detection in a neuronal processing integrated circuit.

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