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An Integrated System for Multichannel Neuronal Recording with Spike / LFP Separation and Digital Output

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***Abstract*— A mixed-signal front-end processor for multi-channel neuronal recording is described. It receives twelve differential-input channels of implanted recording electrodes. A programmable cutoff HPF blocks DC and low frequency input drift. The signals are band-split at about 200Hz to low frequency local field potential (LFP) and high-frequency spike data (SPK), which is band limited by a programmable-cutoff LPF. Amplifier offsets are compensated by calibration DACs. The SPK and LFP channels provide variable amplification rates of up to 5000 and 500, respectively. The analog signals are converted into digital form, and streamed out over a serial digital bus. A threshold filter supresses inactive portions of the signal and emits only spike segments. A prototype has been fabricated on a 0.35μm CMOS process and tested successfully.**

I. Introduction

Recent advances in fabrication of MEMS microelectrode arrays [1], [2], together with the ability of coupling the arrays directly to VLSI chips, allow simultaneous monitoring of hundreds of neurons. Communicating raw neuronal signals from a large number of units results in prohibitively large data rates [3]. When sampled with 20Ksps, eight bit precision, even a hundred of electrodes would generate 16Mbps, too large for common methods of low-power wireless communications. Evidently, some form of data reduction must be applied prior to communication. It is possible to detect the presence of neuronal spikes as demonstrated in [3] and communicate only active portions of recorded signals, which may at best lead to an order of magnitude reduction in the required datarate [4]. Another order of magnitude reduction can be achieved if the neuronal spikes are sorted on the chip and only mere notifications of spike events are transmitted to the host. Power feasibility of on-chip spike sorting is examined in [5]. This work focuses on an integrated neuronal recording front-end with on-chip A/D conversion, designed for further integration with spike sorting.

Prior to performing the A/D conversion, the front-end splits the neuronal firing activity band (SPK) and the local field potential band (LFP) in the analog domain, immediately after the first amplification stage. The two signal bands are processed by separate analog chains and are both made available to the host in digital form. The required data acquisition dynamic range (i.e. ADC precision) is consequently reduced from 10 to 7 bits [4].

A front-end neuronal recording IC has been designed, fabricated on a 0.35μm CMOS process, and tested. The chip contains twelve true-differential input channels, SPK/LFP band separation, on-chip A/D conversion and high-speed serial data communication. The on-chip controller is capable of detecting spikes by means of threshold crossing; it can transmit only the portions of signal containing spike activity. Analog SPK and LFP outputs of every channel are also provided.

II. Architecture

The chip architecture is shown in Fig. 1. The on-chip

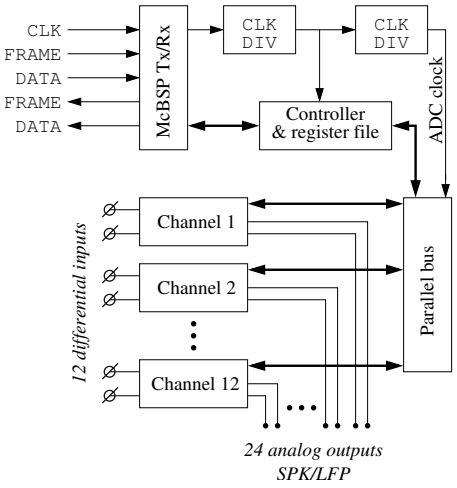

Fig. 1. Chip architecture

controller is responsible for host communication, chip timing, internal register access, channel readout and spike detection. Host communication is carried out over a five-wire serial McBSP [6] bus. Channel registers and A/D converters are accessed through an internal parallel bus.

The controller has two modes of operation, idle and read-out. In the idle mode, contents of internal registers can be exchanged with the host. In the readout mode, the controller

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reads the channel ADCs continuously, checks for threshold crossing events on every channel, and transmits the active signal segments to the host. The controller can operate on the entire set or on any specified subset of the twelve available channels.

A threshold crossing event is triggered for a certain channel when the output of this channel is below the low threshold or above the high threshold. A certain number of samples from that channel will be communicated to the host following the threshold crossing event. Both the threshold values and the number of samples to transmit after threshold event are programmable. If both threshold values are identical, the entire data stream is transmitted.

III. Recording channel

Fig. 2 shows the recording channel block diagram. The input signal is amplified fifty times by the first stage, which also converts the differential signal to single-ended. A first-order RC filter splits the signal into high frequency SPK and low frequency LFP parts. The splitting pole is roughly placed at 200Hz, with a 5MΩ resistor (high resistive polysilicon) and 160pF (gate-oxide) capacitor.

The SPK signal is amplified by an intermediate x10 stage and a variable gain amplifier (VGA) with digitally selectable gain of 2.5, 5, 7.5 or 10. The SPK chain maximal gain is therefore 5000. SPK signal band is limited by a second-order Bessel LPF, implemented as a Sallen-Key biquad [7]. The -3dB frequency is digitally programmable in the range of 8-13kHz, by means of a multi-tap resistor. The LFP signal is amplified by an identical VGA, without the intermediate x10. The LFP chain maximal gain is 500.

Both SPK and LFP channels have to be compensated for DC offsets introduced by element mismatch. The LFP channel amplifies the preamp input offset (hundreds of μV , typically) by 54dB; unless compensated, it would severely degrade the LFP dynamic range or even saturate the VGA. The SPK channel amplifies the offset of the intermediate x10 stage by 40dB, as the preamp DC is blocked by the splitter. Though smaller than LFP, SPK offset is yet significant: the x10 stage has larger input offset compared to the preamp, as the latter uses very large input devices (due to noise requirements). DC offset compensation is carried out by adjusting the VGA reference voltages with a pair of 5bit calibration DACs.

Finally, either one of the SPK or LFP channels is sampled by a Miller-capacitance sample and hold circuit and converted by a 10 bit successive approximation ADC, which incorporates a dual resistor ladder DAC.

A. Input preamp

Voltage offsets inherent to neural signal recordings constitute a major challenge in preamplifier design. An input signal must be high-pass filtered at frequencies as low as several Hertz, to let the LFP signal pass unsuppressed. Such time constants are not readily available in integrated circuits.

Off-chip elements are sometimes employed at input stages [4], [8]. Several fully integrated approaches were also demonstrated: The signal can be capacitively coupled to the amplifier using the polarization capacitance of the electrode, shunt either by a weak-inversion MOS transistor [9] or a reverse-biased diode [10], both delivering a large small-signal impedance to form a low frequency pole at the input. In the former, the gate bias of the shunting transistor is derived with a laser-trimmed resistor. The DC gain of this scheme is not a strict zero, since the real part of the electrode impednace, although very large, is not infinite. DC gain is therefore defined by the ratio of the shunting resistance and the parallel resistance of the electrode.

Another fully integrated approach suggests using a pseudo-resistor device based on a weak inversion MOS and a parasitic bipolar [11], [12], [13]. Such a device has an extremely large small signal resistance at small bias voltages.

Our preamp schematic is shown in Fig. 3. A differential stage with a gain of five and an HPF filter is followed by a differential-to-single-ended stage with a gain of ten. The total preamp gain is therefore 50.

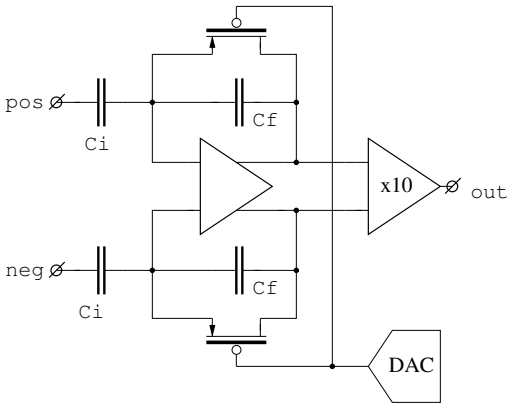

Fig. 3. NPR03 preamp

The minimal gain to be provided by the preamp is determined by noise constraints as follows. RMS noise introduced by the frequency splitter resistance into the SPK signal (band of 10kHz) is:

$$\sqrt{4kTR \cdot 10^4} = 28\mu V$$

The preamp must provide gain well above 20dB to keep the splitter contribution below the target 2μV .

We have chosen to place a weak inversion MOS transistor in parallel with C_f, to provide a first order high-pass filter for input DC suppression. The cutoff frequency is digitally programmable through gate bias voltage adjustment with a calibration DAC. As the conductance provided by the feedback transistor does not belong to a set of controlled process parameters, we have measured a significant variability (up to an order of magnitude) in cutoff frequency among the channels, even on a same die. Being able to control the gate bias voltage, we have managed to calibrate all channels to a 1Hz cutoff.

Given a single pole splitter with pole frequency f_1, the noise energy contributed by the feedback resistor to the SPK signal

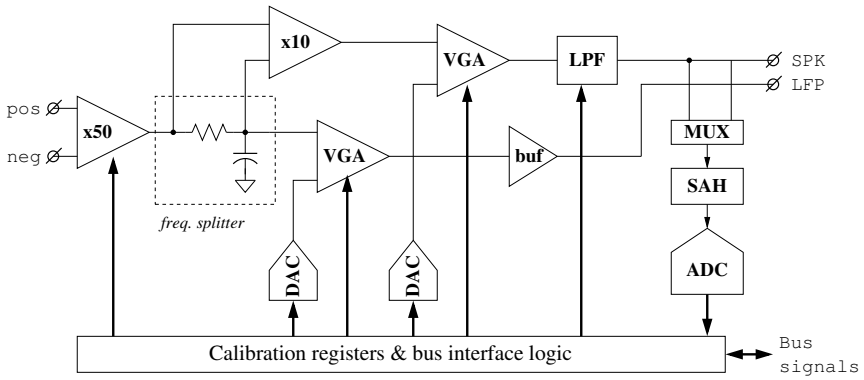

Fig. 2. NPR03 recording channel

is:

$$\int_0^\infty \frac{4kTg}{\omega^2 C_f^2 + g^2} \times \frac{\omega^2}{\omega^2 + \omega_1^2} d\omega$$

Assuming f_1 (about 200Hz) is much larger than the selected cutoff frequency f_0 of the input HPF, the expression above can be re-written as:

$$\frac{kT}{C_f} \times \frac{\omega_0}{\omega_1}$$

and reflected to the input as:

$$\frac{kT}{C_f} \times \frac{\omega_0}{\omega_1} \times \left(\frac{C_f}{C_i}\right)^2$$

Placing the resistive element in the feedback has an important advantage: the noise generated by the resistor is attenuated by the amplifier gain. For f_0 of 1Hz, f_1 of 200Hz, first stage gain of five and C_f of 500fF, we obtain about 1.8μV input RMS noise (remembering that there are two resistive elements in a differential stage). The calculations did not include the opamp noise.

Another important tradeoff is revealed by the above formula: the higher the f_0 selection, the higher the noise contribution of the pseudo-resistors; yet the better the DC rejection. In that context, providing for a selectable cutoff frequency is another advantage.

IV. Measured results

A 0.35μm CMOS double poly, quad metal IC was fabricated and tested electrically. The input high-pass filters were successfully brought to the cutoff frequency of 1Hz. Fig. 4 shows the LFP step response for different settings of gate bias DAC. Without calibration, a large channel-to-channel variability was indeed measured: variations of almost two decades can be observed on Fig. 5, showing cutoff frequencies of several channels for different settings of input DACs. Test results are summarized in Tab. I.

V. Summary

A mixed-signal processor for multi-channel neuronal recording has been presented. It receives twelve differential-input channels of implanted recording electrodes. The signals are split at about 200Hz to low frequency local field potential (LFP) and high-frequency spike data, band limited by a programmable-cutoff LPF. Another programmable cutoff filter eliminates the DC component at the input. Amplifier offsets are compensated by means of calibration DACs. The SPK and LFP channels provide variable amplification rates of up to 5000 and 500, respectively. The two outputs per each channel are converted into digital signals, and the digital controller produces a serial stream at up to 8Mbps. The controller can

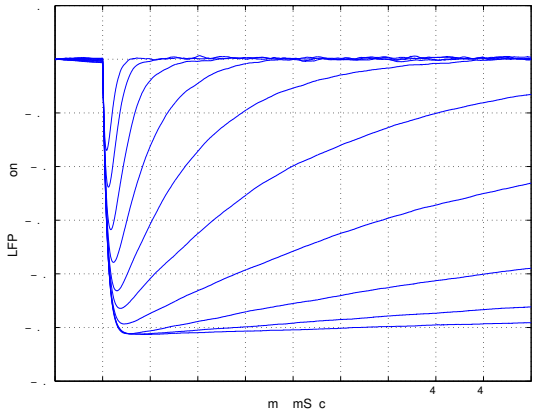

Fig. 4. LFP step response for different input HPF DAC settings

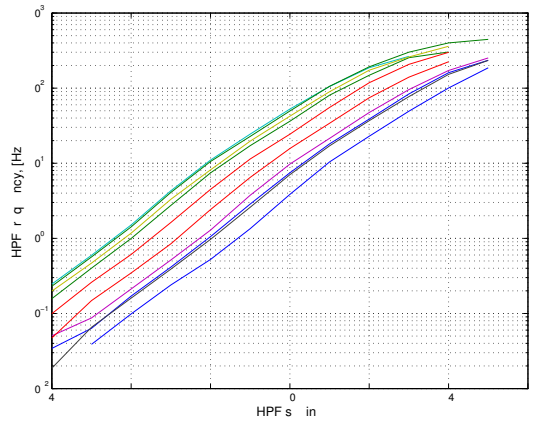

Fig. 5. Input HPF cutoff vs. DAC setting, several channels

TABLE I

TEST RESULTS SUMMARY

SPK gain	3780
SPK noise (RMS)	3μV
LFP gain	430
LFP noise (RMS)	6.6μV
Split frequency	350Hz
Channel power consumption	1mW
ADC INL	1.5 LSB
ADC DNL	0.8 LSB

also apply a threshold filter to supress inactive portions of the signal and emit only spike segments, thus potentially reducing the required communication bandwidth. A prototype of the processor has been fabricated on a 0.35μm CMOS process and tested successfully.

ACKNOWLEDGEMENT

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