Low cost CMOS multi-electrode arrays

Alex Lyakhov[1], Yevgeny Perelman[2], Ran Ginosar[2], Shimon Marom[3]

(1) Intel Corporation, Haifa, Israel
(2) Technion – Israel Institute of Technology, Faculty of Electrical Engineering, Haifa, Israel 32000
(3) Technion – Israel Institute of Technology, Physiology, Faculty of Medicine, Haifa, Israel 32000

CMOS Multielectrode Arrays with and without post-processing

Glass-substrate Multi-electrode Arrays (MEA) have become a valuable tool in neurophysiological research and drug screening. CMOS technology is a promising platform for the development of next generation MEAs. It can enable a substantial increase of the spatial density to over a million electrodes. Tight integration of the recording probes and the amplifying circuitry can also enhance noise immunity in CMOS MEAs. Finally, entire data-processing algorithms can be integrated on the same die with the recording electrodes.

Fabrication of CMOS microelectrode arrays reported so far employed a standard CMOS process followed by custom processing steps to protect the recording electrodes (typically aluminium) from corrosion in the physiological solution. While fabrication of CMOS is widely available, post-processing steps make CMOS MEAs proprietary and expensive: A special microelectronic processing facility is required, and lithographic mask sets impact the cost.

We have examined the feasibility of fabricating MEAs using a standard CMOS process with no post-processing steps. It was established that neurons can be successfully cultured, with firing activity recorded for several weeks on a standard CMOS die with no electrode coating. Stimulating neuronal tissue with current, however, has not succeeded, due to the high corrosion rate of aluminium under electric stress. To facilitate stimulation in low cost MEAs, we investigate simple post-processing steps that do not require lithography.

CMOS Multielectrode Array Test Chip

A CMOS MEA test chip was fabricated with a standard 0.35μm mixed signal CMOS process (Fig. 1). It was encapsulated in a 120-pin ceramic package, with a round glass bath mounted on top of the die (Fig. 2). The chip included circuitry for DC stabilization of the electrode potentials, analog amplification of the recorded signals, analog buffering of the amplified signals out of the chip (Fig. 3) and temperature control. Bonding wires were isolated with Sylgard-184 (Fig. 4). EpoTek epoxy isolation was also tried, but resulted in cracks (Fig. 5) that damaged the bond wires.

The chip was tested electrically and found completely functional. Dielectric electrode coatings (not requiring lithography) of various combinations of Al_2O_3, TiO_2 and HfO_2 were applied with an electron beam gun evaporator to several dies. Electrical stress tests were carried out on the dies in a biological solution to verify immunity to electrode corrosion (Fig. 6). Coated electrodes have shown significantly better corrosion immunity under stress. However, several tested electrodes have performed very unevenly. This was related to the non-uniformity of the evaporated dielectric layer (Fig. 7, 8).

Rat cortical neurons were cultured on top of the uncoated test chip for six weeks (Fig. 9). Neuronal signals have been successfully recorded once every two weeks (Fig. 10, 11). After about six weeks some electrodes have deteriorated.

In conclusion, it may be feasible to conduct short term neurophysiological experiments on low cost uncoated CMOS MEAs. Further study is required for low cost non-lithographic thin isolation coating.

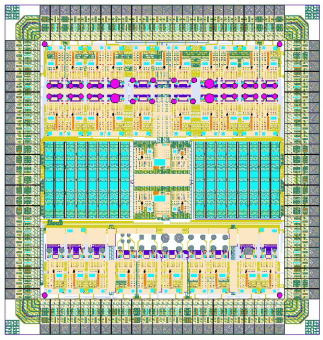

Fig. 1. CMOS MEA test chip layout

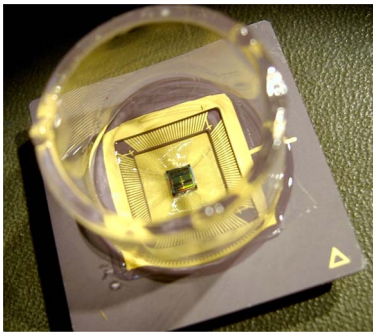

Fig. 2. Packaged chip with a glass bath

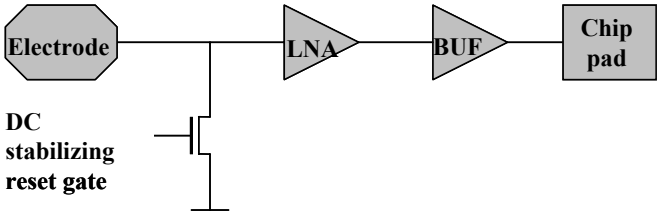

Fig. 3. Circuit diagram

Fig. 4. Sylgard-184 isolation

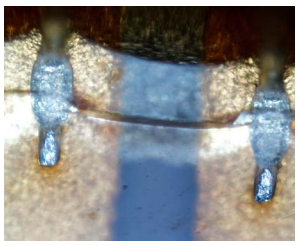

Fig. 5. Epoxy isolation cracks

Fig. 6. Electrode corrosion

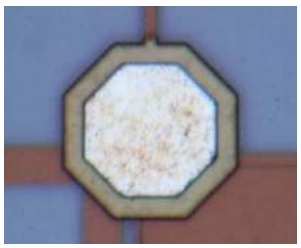

Fig. 7. Coated electrode

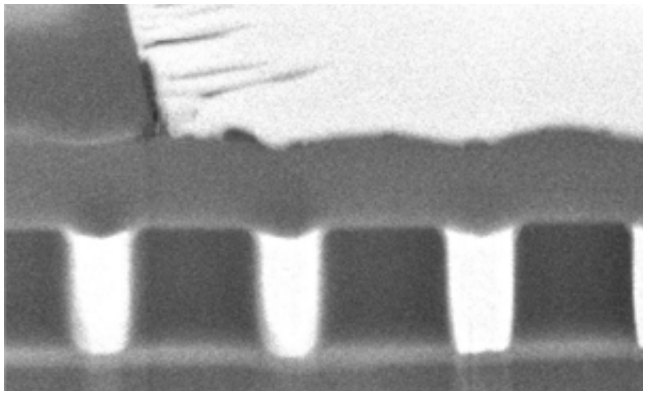

Fig. 8. SEM photo, electrode

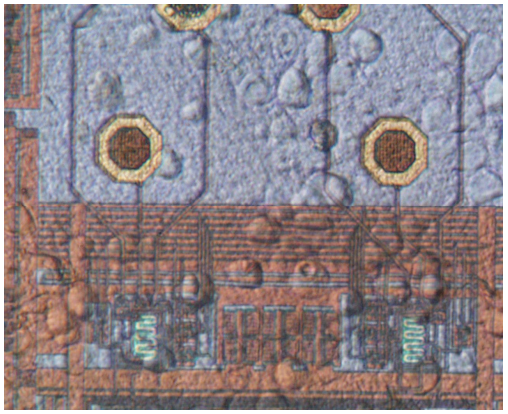

Fig. 9. Neurons on the chip

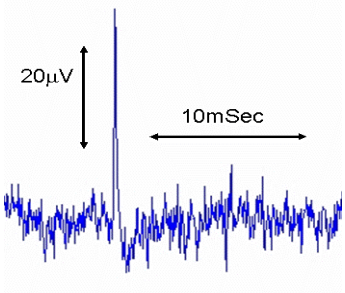

Fig. 10. Recorded spike sample

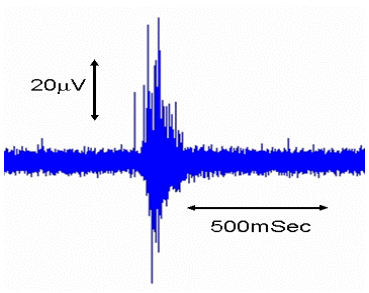

Fig 11. Recorded burst sample