A Wide Dynamic Range CMOS Image Sensor

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We employ Adaptive Sensitivity™ to acquire images at a wide dynamic range. The integration time of each pixel is adjusted according to the intensity of light incident upon that pixel. The integration control circuitry is distributed: A minimal part of it resides in each pixel, and the larger part is on-chip but outside the imaging array. In the past we have demonstrated such circuits on CCD two-dimensional arrays [1] and on TDI sensors [2]. In this paper we present a new architecture, implemented on a CMOS imaging array.

Each pixel contains, besides the photodetector and an output amplifier, a conditional reset circuit and a one-bit flip-flop (Fig. 1,2). Each pixel has a choice of two possible integration times ('long', lasting the entire frame time of 30 msec, and 'short', being 1/16 in length, approximately 2 msec). The control bit stored at each pixel determines that pixel's integration: Long on '0' and short on '1'.
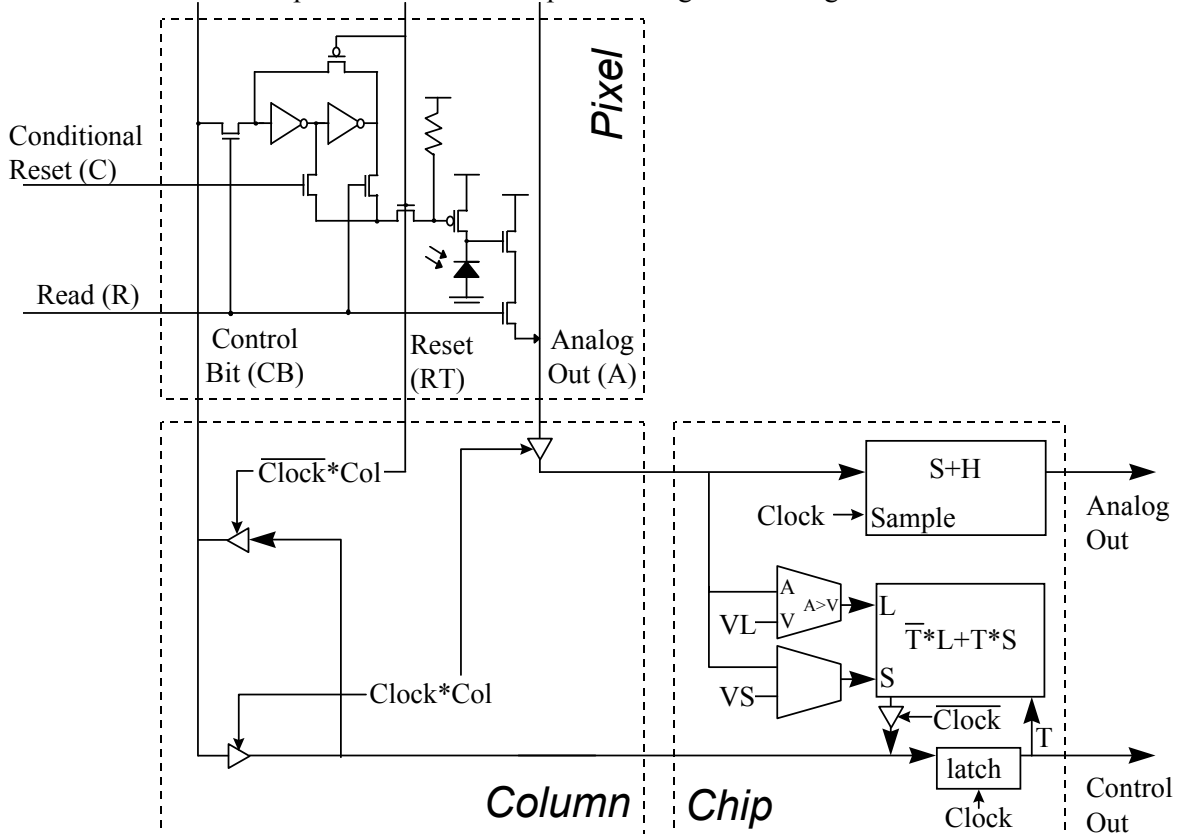

Fig. 1: Pixel, column and output circuits. The pixel comprises 13 transistors, a photodiode, and 7 interconnects (two of which are supplies). A single '1' bit cycles through the columns (at pixel clock rate), making Col=1 in exactly one column at a time. When Clock=1, the pixel value and the control bit are read and sampled. When Clock=0, the new control bit is written back to the pixel, and enabled pixels are reset.

The chip operates in a 'rolling' mode: The frame period of each row is slightly shifted relative to the next row. The row that is presently read out is marked 'A' in Fig. 3, and the 'A' row progresses downwards. RC=10 for the 'A' row. During the first 15/16 part of the frame period, each pixel is conditionally reset every pixel clock cycle (the rows marked 'B' in Fig. 3, for which RC=01). During

the remaining $1/16^{th}$ of the frame (the rows marked 'C') RC=00 and the pixel only integrates. The vertical scan circuit coordinates the downwards progression of the three row types and the corresponding R, C values.
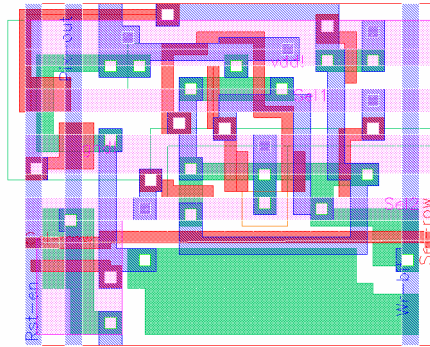

Fig. 2: Pixel layout. The experimental pixel is 60×70 microns at 2 micron technology and fill factor is 13% (substantially smaller pixel and better fill factor are possible when using an advanced technology, such as 0.25 micron).
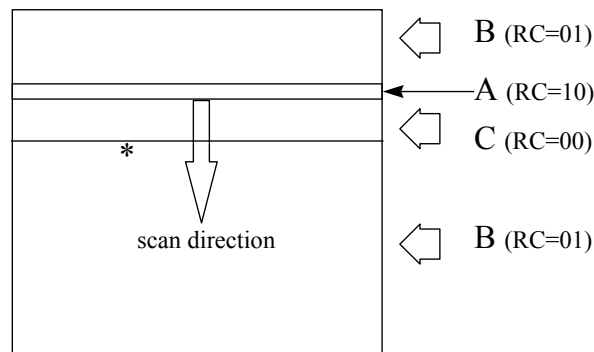

Fig. 3: Row A is being read out. All rows marked B are conditionally reset (those pixels in rows B having '1' stored in their control bit are reset on every clock). The last row B (marked *) will be read out in 1/16 of the frame time. Rows C integrate charge without any reset.

Fig. 4 shows pixel charge integration in both cases of long and short integration. In the former case, charge is integrated throughout the frame time, and the pixel is reset after its value is extracted. In the latter case, the pixel is repeatedly reset (thus avoiding saturation and blooming) until 2 msec prior to termination of the frame period.

The row selected for readout is read one pixel at a time (as controlled by the horizontal scan circuit). The pixel value is compared with Vlong and Vshort thresholds at the output circuit (Fig. 1,5). If the value of a long-integrated pixel is above Vlong, a '1' is written back into its control bit, so that it integrates over a short period on the next frame. Similarly, a low value changes a short pixel into a long one. The two thresholds (e.g., 240 and 10) are spread more than ×16, so as to avoid oscillations due to image variance and noise.

Fig. 6 shows pixel simulation. On the left, a 'short' pixel and its control bit are read out during the first phase of the readout clock cycle. It is reset, and converted into 'long', during the second phase. On the right, a 'short' pixel is reset during a conditional reset cycle.

The inherent dynamic range of each photodetector is approximately 48dB (it may actually be wider, but we convert the value into 8 bits). The pixels with 1/16 shorter integration time also cover a 48dB range, but this range is shifted by 24 dB (×16) relative to the longer integration (Fig. 5). Thus, the total dynamic range is 48+24=72dB. The 1/16 ratio is actually a programmable parameter: The short

integration time can be programmed as 1/4, 1/16, or 1/64 of the long (30 msec) integration time. In the latter case, the full dynamic range is 48+36=84dB. Wider ranges are feasible, either by enabling shorter integration or by enabling three different choices of integration time per each pixel (requiring a different architecture).

Charge

Frame

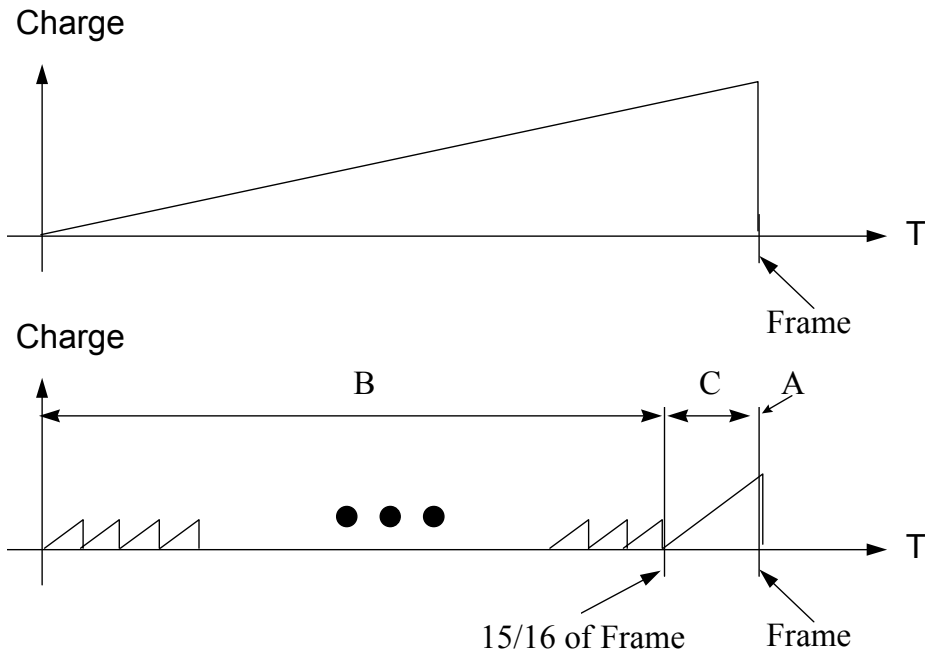Charge

B   C   A

15/16 of Frame   Frame

Fig. 4: Schedule of two sample pixels. The first has '0' in its control bit. It is reset at read-out time, and integrates during the entire frame time. The second has '1' in its control bit. It is reset repeatedly for 15/16 of the frame time (B type rows), and integrates over the remaining 1/16 of the frame (C rows).

72 dB

48 dB

Long Integration

Vshort = 10

Vlong = 240

Short Integration

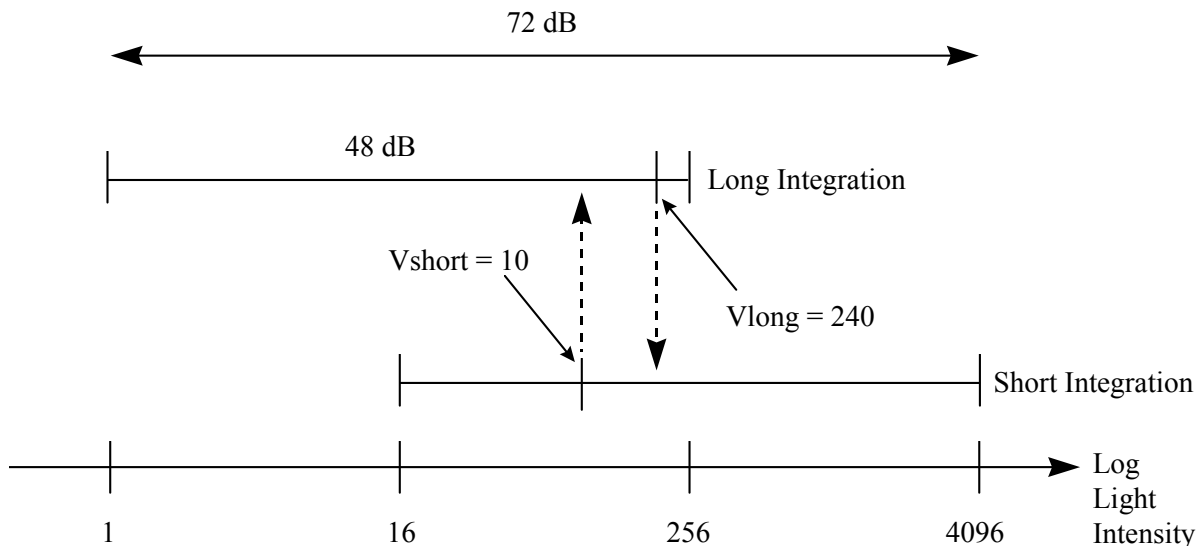Log Light Intensity

1   16   256   4096

Fig. 5: Long and short integration times. While each spans 48dB, their combination covers 72dB. Threshold values affect change of integration times. Units represent relative light intensities.

An alternative architecture (advocated in [1]) employs a memory array in the controller where all the individual control bits are stored. While improving fill factor (there are less transistors per pixel inside the imaging array), the down side of that scheme is the need for a wider access bandwidth to the array.

A 64×64 prototype chip has been fabricated recently (Fig. 7). Early tests have not yet resulted in operational chips by the time of this writing
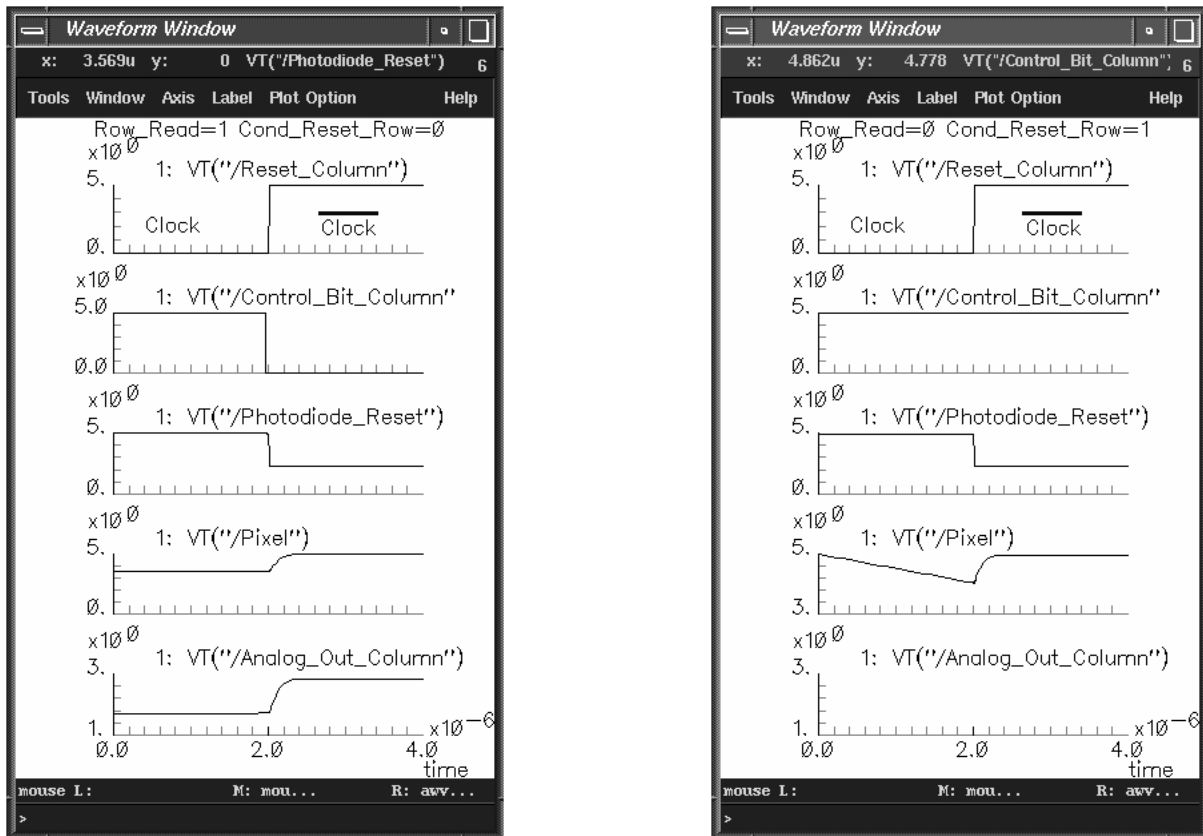

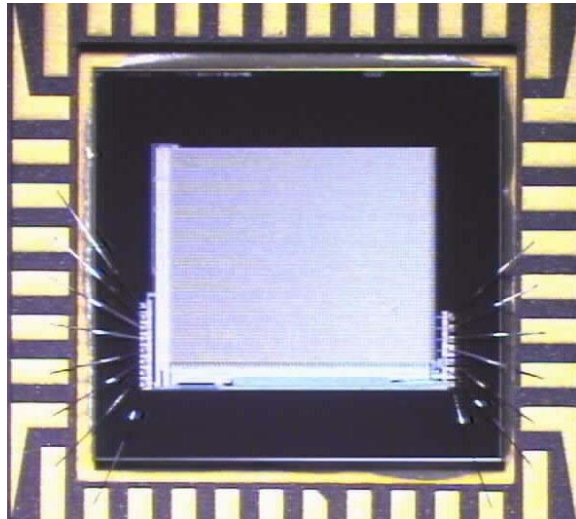Fig. 6: Pixel simulation during read out (left) and conditional reset (right).

Fig. 7: 64×64 2 micron CMOS prototype chip photograph. Horizontal scan and output circuits are at the bottom, vertical scan on the left.

[1]   S. Chen, R. Ginosar, ``Adaptive Sensitivity CCD Image Sensor,'' *CCD and Solid Sate Optical Sensors V,* Proc. SPIE Vol. 2415, San Jose, CA, Feb. 1995.
[2]   S. Chen, R. Ginosar, ``Adaptive Sensitivity TDI Image Sensor,'' EurOpto / SPIE Conf. Advanced Focal Plane Arrays and Electronic Cameras, Berlin, Germany, Oct. 1996.