Front-side bombarded metal plated CMOS electron sensors

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ABSTRACT

Electron detector arrays are employed in numerous imaging applications, from low-light-level imaging to astronomy, electron microscopy, and nuclear instrumentation. The majority of these detectors are fabricated with dedicated processes, use the semiconductor as a stopping and detecting layer, and utilize CCD-type charge transfer and detection. We present a new detector, wherein electrons are stopped by an exposed metal layer, and are subsequently detected either through charge collection in a CCD-type well, or by a measurement of a potential drop across a capacitor which is discharged by these electrons. Spatial localization is achieved by use of two metal planes, one for protecting the underlying gate structures, and another, with metal pixel structures, for two-dimensional detection. The new device does not suffer from semiconductor non-uniformities, and blooming effects are minimized. It is effective for electrons with energies of 2-6 keV. The unique structure makes it possible to achieve a high fill factor, and to incorporate on-chip processing. An imaging chip implementing several test structures incorporating the new detector has been fabricated using a 2 micron double-poly double-metal process, and has been tested inside a JEOL 6400 electron microscope.

Keywords: electron detectors, radiation detectors, sensors, image intensifiers, low light level imaging

1. INTRODUCTION

Electron detectors are used in a wide array of applications, including night vision instruments, electron imaging systems in electron microscopes, biological and medical imagers, and radiation cameras on spacecraft. Solid-state electron detectors have traditionally used Charge-Coupled Devices (CCDs) in two configurations.[1,2] Image-intensified CCDs (ICCDs) project a scene on a photocathode, generating photoelectrons, which are proximity focused onto a Micro-Channel Plate (MCP) whereby their flux is multiplied. The electrons are accelerated onto a phosphor screen, by means of which the electrons are converted to light. Fiberoptic tapers then carry the light to a CCD array, where it is converted to charge, integrated over time and processed. The numerous stages of the detection process manifest themselves in a poor signal to noise ratio. Moreover, the phosphor screen slows down the response time, and the MCP together with the fiberoptic taper degrade the modulation transfer function (MTF) of the resulting picture.

Another common configuration is thinned electron-bombarded CCDs (EBCCD), where many of the steps described above are eliminated. The EBCCD is incorporated into the vacuum tube with the photocathode. The emitted electrons hit the back side of a CCD chip, creating electron-hole pairs which traverse the substrate, amplified by electron-bombarded semiconductor (EBS) gain, on the order of one thousand, depending on incident electron energies. After reaching the well of the CCD, charge is processed in the usual manner. EBS gain is much less noisy than MCP noise.

EBCCDs are often characterized by incomplete energy dissipation in the active material, blooming, and damage to the CCD[3]. Another serious problem encountered by EBCCDs is the formation of a positive electric field at the back side of the chip[4], leading to loss of signal by surface recombination of electrons with holes. The chip must be thinned to a thickness of approximately 10-15 μm, resulting in reduced yield and an increase in manufacturing cost[2].

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Front-side electron-bombarded virtual phase CCDs have been described[5]. However, these devices suffered from radiation damage due to charge build-up in the oxide layer. The damage manifested itself in flat band shifts, and consequently in a shift of the required voltages for charge transfer.

The semiconductor electron detectors described above suffer from non-uniformities in the silicon, which translate to a fixed-pattern noise in low light level applications. Moreover, their gain is dependent on the spectrum of the incident particles, namely on the ratio between incident energy and the work function of the semiconductor, thus producing a signal that is dependent both on flux and energy. Their read-out speed is limited by the charge transfer mechanism, and for very fast imaging applications, such as real-time beta radiography imaging of chemical reactions, detection pixels are bump-bonded to electronic read-out pixels in order to speed up read-out times, consequently reducing resolution and increasing cost[4]. Furthermore, the CCD process makes it difficult to have on-chip image processing.

This paper proposes a new electron detector and a pixel structure incorporating the detector. The detector answers some of the issues described above, using a standard MOS technology. It is based on the short stopping distance of electrons in metal, and utilizes a metal layer on the surface of the chip both as a protective layer and a detecting layer. Because of this protective layer, and since a much higher yield is expected once mechanical processes are eliminated, much more complex processing, both on-chip and inside the pixel may be incorporated. As a result, the expected lifetime of the sensor is extended, and the density, uniformity and dynamic range of the resulting image are expected to improved.

The next section explains the concept of the new detector. Section 3 describes various pixel configurations of the new detector. Finally, section 4 presents experimental results of a test chip incorporating the new detector structure.

2. THE NEW DETECTOR CONCEPT

Complicated circuitry in front-side bombardment CCD chips has traditionally been ruled out because of the effect of charge accumulation in the gate oxide, which increases the dark current[7] and consequently precludes the electrical operation of devices in the chip within seconds[6]. The present device incorporates metal layers which both protect the underlying gate structures and detect electrons.

When electrons collide with a target, they scatter electrons inside it. The volume from which scattered electrons may be re-emitted from the surface is called the interaction volume. It has been shown[8] that for incident electrons with energies ranging from 10 eV-1000 keV, the maximum range, defined as the distance from the surface to the bottom of the interaction volume is given by:

$$R = \frac{2.761 \times 10^{-11} A E_0^{5/3}}{Z^{8/9} \cdot \rho} \qquad (1)$$

where E_0 is the incident electron energy, A is the atomic mass in a.m.u., Z is the atomic number and ρ the density in $g \cdot cm^{-3}$. Assuming aluminum density $\rho=2.7\ g \cdot cm^{-3}$, then for incident energies in the range 2-6 keV electrons are completely stopped after 90 - 560 nm. respectively[9,10]. From Orbit Semiconductor's process specification values for sheet resistance of the two metal layers in their 2μm process, we calculated a metal thickness of 540 and 900 nm for metal layer 1 and 2, respectively. Thus, electrons up to approximately 6 keV will not penetrate either of the metal layers.

When electrons are absorbed in the metal layer, they negatively charge that layer. The concept behind the various detectors presented here is the detection of this change in net charge. The metal detection layer may be used in several different configurations (see Fig. 1): as a conductor connected to an ammeter; as an input node to a CCD; as a capacitor plate; or as the input node of a transconductance or transimpedance amplifier.

The ammeter implementation of the electron detector mimics the absorption current measurement mechanism in electron microscopes, where the conductive sample holder is grounded through a pico-ammeter. In its VLSI rendering, the metal pixel is connected to ground through an ammeter. In case of an array structure, sampling may be achieved through a transistor that grounds the pixel when inactive. While simple and very area-efficient, this configuration is inadequate for a noisy environment, because the electron current is not amplified. Moreover, since it operates in current-mode, versus integration-mode, its sensitivity is less than that achievable in other configurations.

When used in a CCD-type array, the collecting metal pixel is connected to the bulk through a diffusion (Fig. 1b). Collected electrons are pulsed into the potential well under electrode f_1 by pulsing the input gate beyond a voltage threshold[11]. From this point, charge is processed similarly to regular CCDs. This configuration may be juxtaposed to existing electron-bombarded CCD chips, and can utilize existing CCD architectures. However, since EBS gain does not take place, this implementation suffers many of the drawbacks of regular CCD electron detectors, such as limited frame rates, with inferior sensitivity.

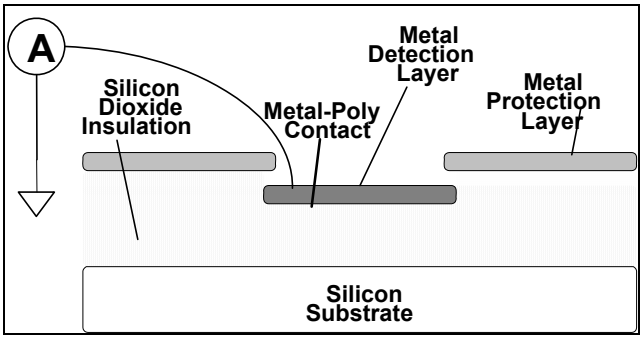


Figure 1a: Cross section of the detector connected to an off-chip ammeter

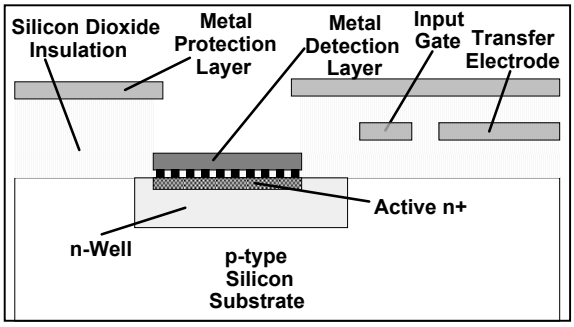


Figure 1b: Cross section of the detector in a CCD configuration

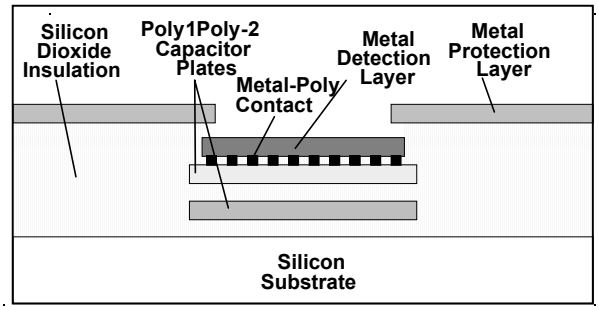


Figure 1c: Cross section of the detector in a capacitor configuration

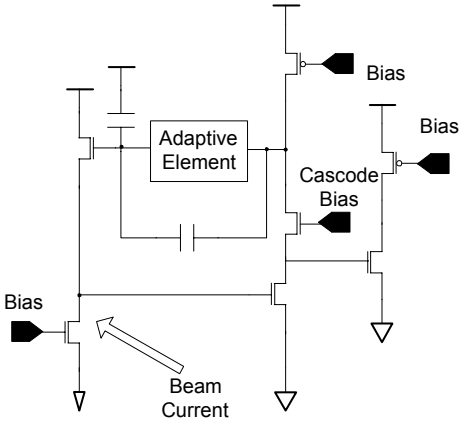


Figure 1d: A continuous, adaptive detection configuration incorporating the detector

The preferred incorporation of the electron detector into a pixel is through a capacitor. The metal detection layer is connected to a polysilicon layer, acting as the top plate of a capacitor (Fig. 1c). During the precharge phase, the top capacitor plate is charged to a positive voltage. After precharge is complete, the capacitor is disconnected from the supply and is set to float. Incident electrons lower the voltage on the capacitor plate at a rate $dV/dt = F/C$, where F is the electron flux [Coulomb/sec] and C is capacitance (Farad), assuming capacitor linearity, as in the case of poly-poly capacitors.

In contrast with a CCD-type device, data is continuously available. It is sampled through a read-out transistor, which is included in every pixel. An added feature of the capacitor-type pixel is the option for an active pixel setup, with in-pixel amplification. Read-out of data may be done in parallel at very high rates, thus alleviating many of the problems associated with CCD serial read-out. Resetting of the capacitor voltage may be carried out either globally for the entire pixel array, or individually, according to the incident electron flux[12].

A different scheme applies the metal electron-detecting pixel as a current input node to an in-pixel amplifier. As an example, we altered an adaptive pixel structure, previously used with a photodiode structure[13], to implement the electron-detecting device. The reverse-biased photodiode had been replaced by the electron detector, acting as a negative current source, in series with a biasing resistor (Fig. 1d). The advantage in this scheme is its generality, because for all practical purposes, any current-to-voltage or current-to-current amplifier may be used, as the application requires.

In order to spatially localize the electron signal, the metal pixels are separated by a second metal protection layer (Fig. 1) which is connected to a positive supply, such that any electrons hitting this metal are swept to that supply. This separating metal also protects the underlying oxide from electrons that reflect from the surface at an angle, by providing a protrusion over the oxide. Thus, blooming, which is a potential drawback of traditional backside bombarded CCDs, is virtually removed.

One important difference between back-illuminated CCDs and the Metal-plated Front-side-bombarded Electron Detector (MFED) is that in the former, EBS occurs. Since MFEDs merely absorb incident electrons, no gain process takes place. In case of a high flux of electrons in the relevant energies (2-6 keV), there is no need for additional components in the system. However, for low light level applications, a micro-channel plate may be used. A MCP is composed of millions of thin fibers, which emit electrons in response to either photons, charged particles or neutrons, and amplify them, up to eight orders of magnitude in some configurations[14,15]. Thus, MFEDs may be used as an X-ray, neutron, photon, or as a charged-particle detector. Because of the poor S/N of existing MCPs, the MFEDs should be operated without MCPs when possible, taking into account such criteria as cost, resolution, response time, size, dynamic range and on-chip processing requirements.

In standard MOS processes, the detecting and protecting layers are made of aluminum. Electrons which are trapped in an insulating layer cause charge-up of that layer. It is therefore desirable to avoid the formation of an oxide layer over the aluminum. Operation of the detector in a vacuum environment, which is used in almost all existing electron detecting systems, will greatly reduce oxidation. Oxidation may be overcome altogether by using an inert metal, such as gold, which allows for higher beam energies[16].

3. TEST CHIP PIXEL CONFIGURATIONS

In order to evaluate different pixel structures, we designed a test chip with various structures. A double-poly double-metal 2μm process was chosen for two reasons: it is the technology with the largest feature-size currently available from MOSIS and thus has the thickest metal layers, and its double-poly structures are best suited for the linear capacitor approach. The test structures are to prove the detection concept, measure detection efficiency and dynamic range, and measure the noise associated with each of the pixels, so that an optimal array chip may be designed later.

All structures were designed for maximal simplicity and robustness. Detector capacitance exceeds 250 fF, so that parasitic capacitance becomes negligible. For preliminary testing, we have assumed current levels several orders of magnitude above noise levels, so that basic operability may be established. Integration times may vary from several nanoseconds to milliseconds, depending on the beam currents used, so that pixel response, as well as any radiation damage will be measurable for a large range of input currents.

In order to facilitate maximum testability, two sets of almost-identical test structures were designed. One set simulates the incident electrons by drawing current out of the metal pixel, through a built-in, externally adjustable current source, which can draw from 5 pA to 100 μA. Its pixels are covered by the protecting metal layer, isolating them from external radiation. Apart from a current sink, each structure contains an MFED configured in a pixel structure, as described below. In order to drive the output capacitance, a source follower was connected to the output of each pixel. The MFEDs in the second set of test structures are exposed, i.e., the passivation above the metal layer is bared, by drawing a layer of via on top of the metal, thereby eliminating oxide growth, and adding an "overglass" layer, which removes the top-most passivation.

In the most straightforward test structure implemented in the chip, the metal detecting layer is connected by ohmic contacts to the top plate of a polysilicon-polysilicon capacitor (Fig. 1c, 2a). The circuit schematic of the pixel incorporating this structure is shown in Fig. 2b. During the precharge phase of each clock cycle, a reset signal sets the capacitor voltage to a pre-charge level. At the second phase, the capacitor is disconnected from the supply, and incident electrons discharge its voltage. A source follower buffers the capacitor voltage for readout. The in-pixel amplifier may operate in one of two modes. In "analog" mode, the voltage on the capacitor plates is linearly transferred to the output node, with an analog-to-digital converter in a later

stage, in order to determine the voltage drop, and hence the total accumulated charge. In "digital" mode, the amplifier is designed such that it is triggered at a pre-determined voltage. In the latter mode, either a logical "0" or "1" is output, and the time for discharging to the said threshold is indicative of the accumulated charge, thereby greatly simplifying the analog-to-digital conversion.

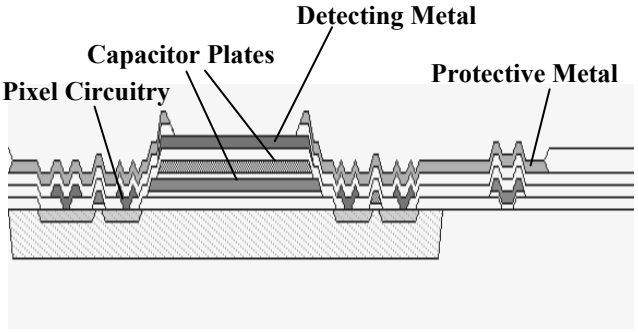


Figure 2a: Cross section of a detector pixel with a poly-poly capacitor structure

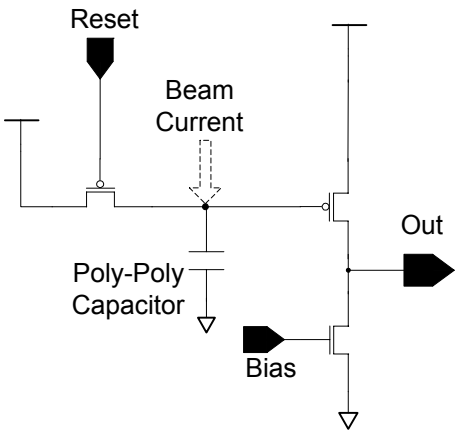


Figure 2b: A detector pixel with a capacitor structure

While a poly-poly capacitor behaves in a desirable fashion, i.e., its capacitance remains constant (independent of voltage), most MOS processes lack a second polysilicon layer. For this reason, a test structure similar to the one above, but using a gate structure for capacitance was designed. Here, capacitance between a polysilicon layer and highly-doped silicon replaces the poly-poly capacitor of Fig. 2a. Obviously, this implementation is less desirable because the capacitance of such a structure depends on the voltage difference across its plates. Two configurations incorporating this structure were implemented. In one, the detecting metal layer lies right above the amplifying circuitry of the pixel. In the second configuration, the metal detecting pixel was placed outside the pixel circuitry, and the latter was covered by the protective metal layer. The latter structure is designed to alleviate any cross-talk effects that may arise from electrons incident above the sensitive circuitry.

The circuit element connected to the metal pixel should not necessarily be a dedicated capacitor. In the test structure shown in Fig. 3a**,** the metal element is tied directly to the gate of the input transistor of a source follower. Figs. 3b, 3c depict the layout of the two configurations.

All of the above schemes usually require correlated-double-sampling, whereby a signal is processed in two phases. In the first, the detector only samples noise, while in the second it detects the signal and noise. Subsequently, the former is subtracted from the latter to produce a relatively "clean" signal. The novel autocorrelating detector makes it possible to achieve a similar result in a single phase (Fig. 4a). A differential pair replaces the single-stage amplifier of the previous pixels. One of its inputs is connected to a metal pixel, while the other input is not. Precharge is conducted as before, charging up both the sampling and reference capacitors to a positive voltage. When both capacitors are disconnected from the supply, the voltage of the reference capacitor is only altered by noise, while the sampling capacitor is discharged by incident electrons, in addition to noise effects. Thus, the differential pair amplifies a "net" signal, thereby replacing the sample-and-hold clocking, logic and circuitry, which is usually implemented in most conventional CCD-type detectors. While this scheme is possible to implement in conventional detector architectures, it typically comes at the expense of reduced fill factor, because two pixel structures are required for each actual detecting element. Since in this detector electrons are absorbed by a metal layer which lies above the pixel circuitry, the fill factor is not reduced - it is actually increased with respect to a regular array (Fig. 4b). This improvement in fill factor comes at the expense of pixel density.

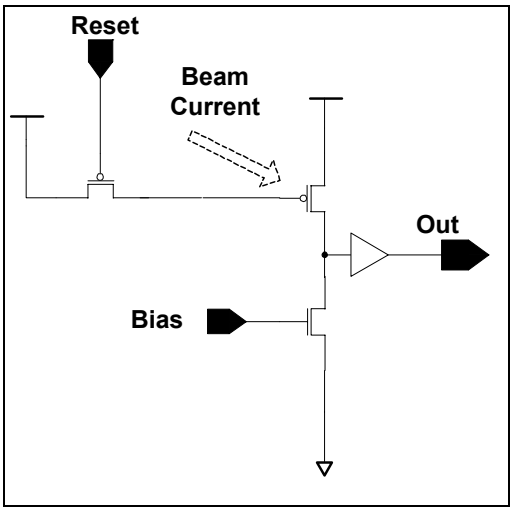


Figure 3a: Pixel schematic of a detector tied to the input gate of a source follower

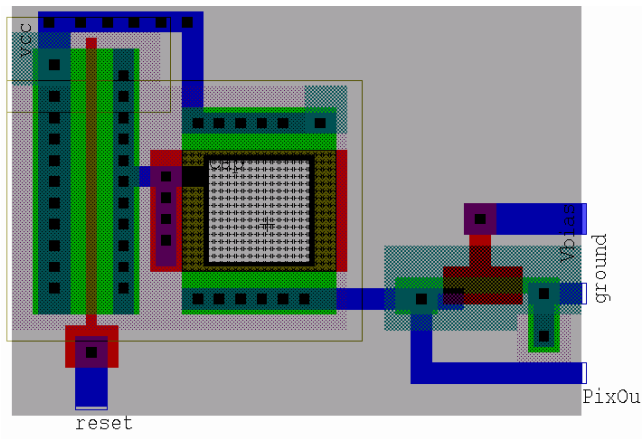


Figure 3b: A common-source-type MFED pixel with overlap between metal detector and pixel circuitry

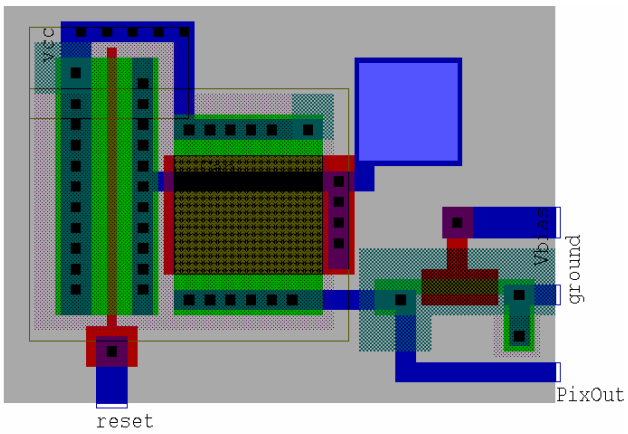


Figure 3c: A common-source-type MFED pixel with non-overlapping metal detector and pixel circuitry

The separation between the detecting and processing layers makes it possible to have in-pixel processing, without sustaining a decrease in fill factor. An adaptive pixel, similar to the one developed by Mead and Delbruck[13] (Fig. 1d) was also included on the test chip. This pixel is especially suitable for night vision systems, which require a wide dynamic range. The circuit mimics the operation of the eye by amplifying small features with a short time constant, and, generally speaking, reducing background illumination changes with a long time constant.

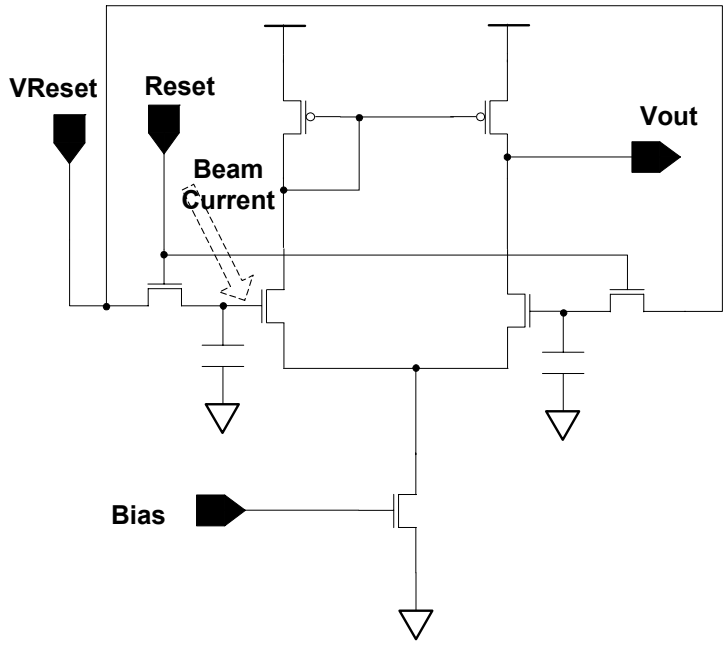


Figure 4a: An auto-correlating electron detector pixel

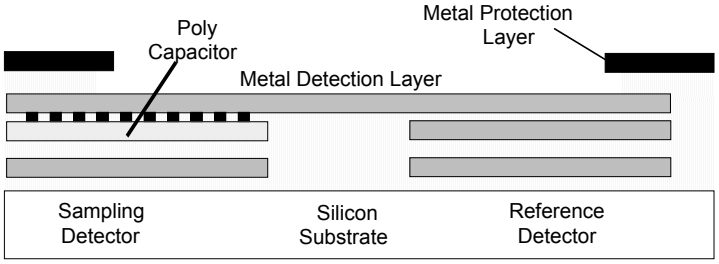


Figure 4b: Cross-section of an auto-correlating detector pixel. Fill factor has been increased relative to CDS schemes.

4. EXPERIMENTAL RESULTS

Two laboratory setups were used to evaluate the MFED test chip – one for carrying out electrical measurements on the structures connected to adjustable current sinks, which mimic electrons, and the other for carrying out the actual tests under an electron beam. The first setup, shown in Fig. 5a, consists of an HP6626A System DC Supply, HP 8116 Function Generator, a Tektronix TDS 724A Digital Oscilloscope, and a Fluke 8010A DVM. A JEOL 6400 scanning electron microscope (SEM) was used to measure the detector response to electrons in variable energies and fluxes. The SEM was equipped with a 40-pin socket feed-through, to allow interfacing with the chip inside the vacuum chamber. A special wiring box was constructed to connect to the feed-through (Fig. 5b).

During electrical measurements it was discovered that the metal plating of the chip act as an antenna. This may result in interference from external sources, such as the AC power supply. However, insertion of the detector into a Faraday cage, or a design using only full rail circuits, such that the output is always differential, counters this problem.

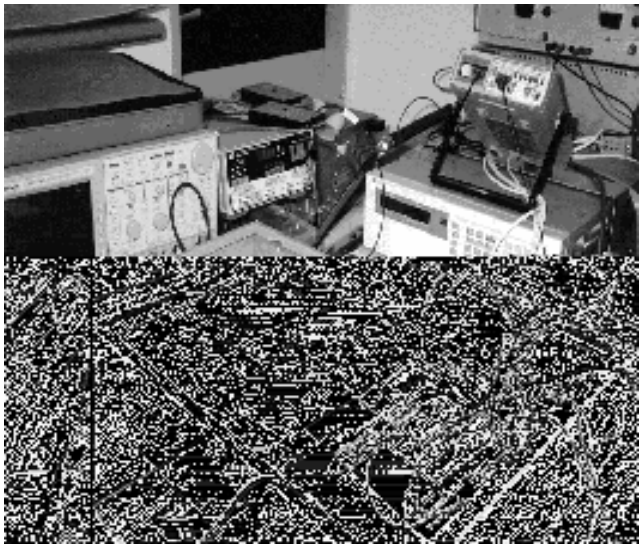


Figure 5a: Laboratory setup for testing the calibration structures of the test chip in the Technion's VLSI Lab

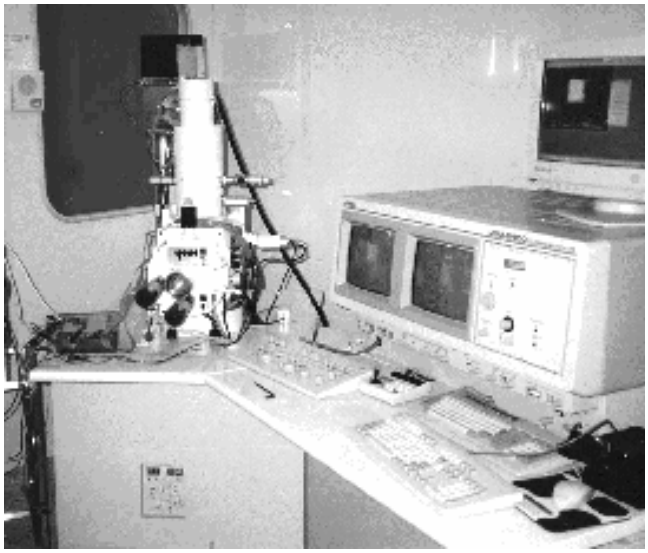


Figure 5b: Laboratory setup for testing the electron detector in the test chip in Technion's Institute for Microelectronics

In order to calibrate the measurements, the adjustable current sinks had to be characterized. This was achieved by measuring the current drawn from the supplies, as a function of the bias on the current sinks. Measurements agreed with SPICE simulation results to within 20%. Deviations may probably be attributed to the fab's deviation from its SPICE parameters. The output buffers were calibrated by setting the reset signal to 5V, thereby maintaining a constant voltage at each of the pixels. The output buffer bias voltage was scanned, and the output voltage recorded. Again, there was close correlation between experimental and simulation results.

Measurements of the capacitor structures were carried out by altering the drawn current, and measuring the time taken by the capacitor to discharge to a pre-determined threshold voltage. The output signal is digital, and the information is contained in the delay between the fall of the reset signal and the switching of the output. Simulation and experimental results are shown in Fig. 6.

As current is drawn from the capacitor, modeling incidence of electrons, its voltage falls until it reaches a threshold, wherein an in-pixel comparator changes the logical output of the pixel. The time difference between end of capacitor precharge and the change in pixel output depends on the precharge voltage, on the threshold voltage of the comparator, and on the electron flux, as well as on the capacitance of the detection node:

$$t = \frac{C\left(V_{pre-charge} - V_{threshold}\right)}{F} \qquad (2)$$

In order to test the electron detector, a tunable electron source was required. The electron energy needs to be adjusted, as well as the electron flux and the position of electron bombardment on the detector surface. Moreover, it is necessary to vary the diameter of the beam, and, for future applications, to scan the beam across the detecting pixels. A JEOL 6400 scanning electron microscope was chosen, and a 40-pin feed-through element was used to electronically interface with the device in the vacuum chamber. The electron energy and current are adjustable, while the bombardment area is simply the field of view.

Since the detector chip is completely covered by an aluminum layer, the chip can "image" voltages. When a detector area is negatively charged, more electrons are repelled by the metal surface and that region seems bright on the SEM image. A positively charged zone emits fewer electrons, thus showing up darker. A negatively charged pixel element, surrounded by positively-charged protective metal is shown in Fig. 7.

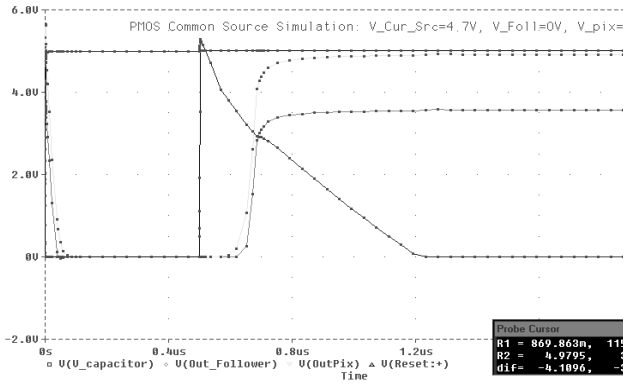


Figure 6a: Simulation results of a gate-poly pixel in digital mode of operation. The capacitor discharges, causing an in-pixel amplifier to switch, and an output buffer converts the signal to 5V, i.e., logical '1'.

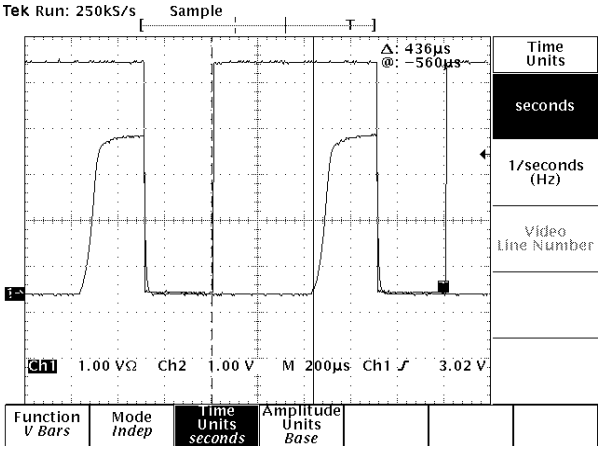


Figure 6b: Capacitor pixel response to discharge current (experimental measurement)

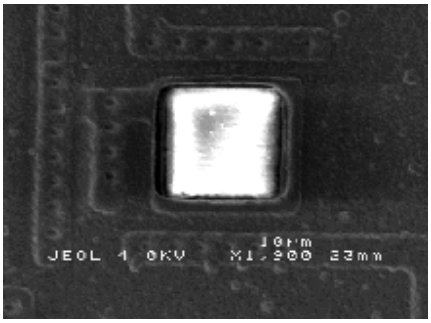
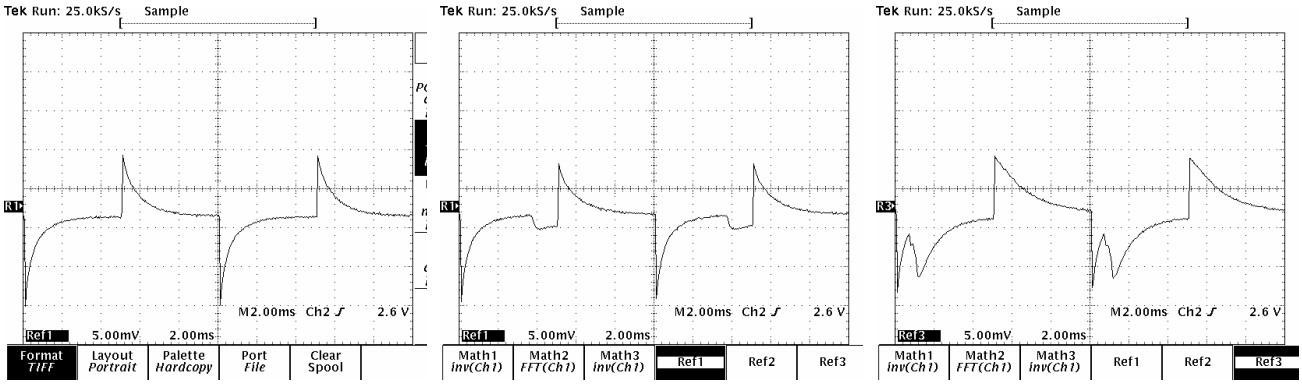


Figure 7: Voltage Imaging: A negatively charged detecting metal surrounded by positively charged protective metal

The electron detector is designed to output a signal depending on incident electron flux. In order to characterize the flux response of the detector, it was bombarded by varying fluxes of electrons, with identical energies and beam diameters. A poly-poly capacitor pixel, with a field oxide layer on top of the detecting metal was put on the test chip in order to investigate the effect of field oxide on the detector's performance. It produced a signal correlating to the incident electron flux. A noisy signal was measured at the output, with a voltage glitch after an average time, t, relating to the incident flux. The pixel response to varying electron currents is shown in Fig. 8a-c.

When the detector is not bombarded by electrons (Fig. 8a), the idle signal is a result of cross-capacitance with the reset signal applied to the gate of the reset transistor. After the cross-capacitance glitch, the capacitor relaxes back to its steady-state voltage. When bombarded by electrons, the output signal becomes noisy, and changes with incoming flux. Figs. 8b-c show averaged pixel responses to 1 and 5 pA currents of 3 keV electrons, respectively. At the beginning of the phase, the cross-capacitance glitch appears as in Fig. 8a. However, after a certain time, a second, negative, glitch shows up. In the case of the 1 pA current, the glitch occurs after 3.8 msec and is 2 mV in amplitude, while for the 5 pA case, the delay is 0.7 msec and the amplitude 6.5mV.



(a) (b) (c)

Figure 8: Output of poly-poly capacitor pixel with field oxide on top of the detecting metal layer: with no electron bombardment (a) with 1 pA 3 keV electrons (b) and with 5 pA 3 keV electrons

We propose that these results suggest a mechanism whereby the field oxide above the detecting metal is negatively charged by impinging electrons. After a certain charge-up time, there is a sudden discharge of the electrons trapped in the oxide into the detecting metal. This may explain the negative glitch in the output voltage.

For a first order approximation, assume a unity gain for the two amplifying stages (in-pixel amplifier and output buffer). Let C be the capacitance of the detecting node, and ΔV the magnitude of the glitch due to impinging electrons. We can calculate the equivalent detected charge:

$$Q_{detected} = C\Delta V = 548fF \times 2mV = 1.096\times10^{-15} \text{ Coulomb} \quad (3)$$

We can also calculate the actual impinged charge:

$$Q_{impinged} = I\Delta t = 1pA\times3.8msec = 3.8\times10^{-15} \text{ Coulomb} \quad (4)$$
$$= 22{,}754\ e^- = 0.29\times Q_{detected}$$

Almost one third of the electrons, which impacted the field oxide over the detecting metal, eventually reached the metal layer and the attached circuitry. We can assume that the remaining electrons were either returned to the vacuum or attracted to the neighboring positively-charged protective metal layer. The detection efficiency in this case is 29%.

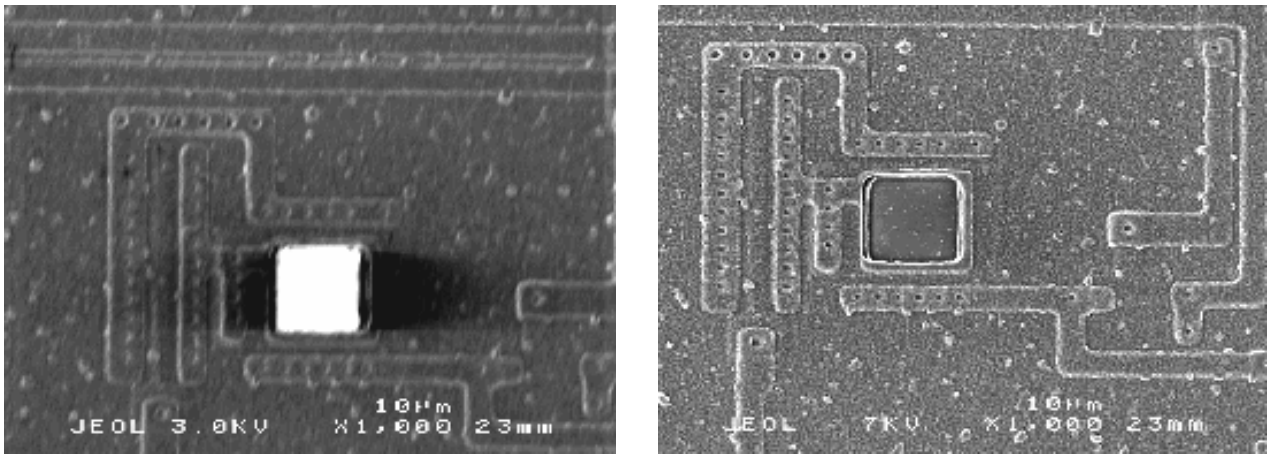
When the electron current is increased to 5 pA, the impinged charge is 20,958 e^- while the detected charge is 16,407, translating to a detection efficiency of 78%. Since the electron energy remained the same, it is improbable that the reason for the increase in quantum efficiency is small reflectivity of electrons. Moreover, approximately the same amount of charge impacted the oxide until discharge, so the reason is not an increased electrostatic field inside the oxide. A possible explanation is that a leakage process takes place, due to the electrostatic field between the oxide and the positively-charged protective metal. Let us define a leakage current:

$$I_{leakage} = (Q_{impinged}-Q_{detected})/t_{discharge} \quad (5)$$

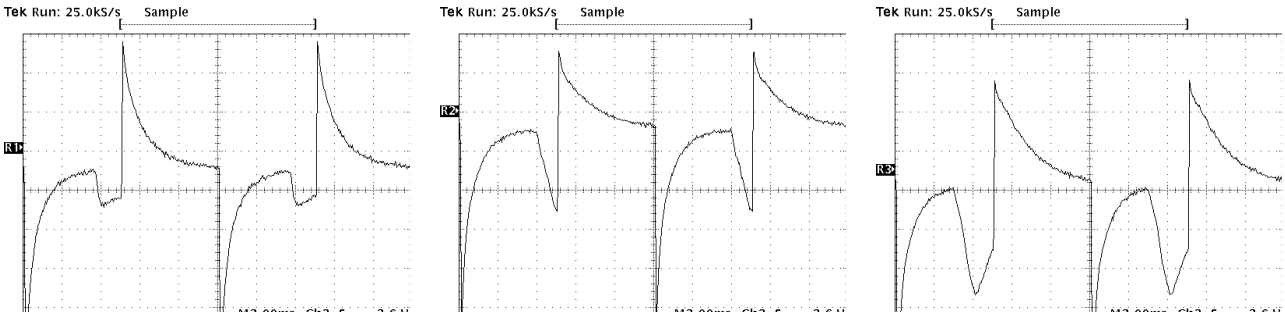
For 1 pA beam current, $I_{leakage} = 0.7pA$, and for 5 pA, it increases to 1.1 pA. These leakage currents are, of course, very high, due to the presence of the oxide layer.

As described in Section 2, incident electron energies affect the detector in several ways. For energies lower than 2 keV, the penetration depth will be low, and many electrons will be reflected back from the metal, thus lowering the detection efficiency.

In the range of 2-6 keV, the electrons will penetrate the metal and the majority of them will be completely stopped in it. In this energy range, as the electron energy increases, the penetration depth increases and a smaller fraction of the electrons are able to escape back to the surface. Therefore, for similar beam currents, as the energy increases, we would expect the detected signal to increase.



(b)



(c) (d) (e)

Figure 9: Electron energy effect on detector quantum efficiency: When the detector is bombarded by 3 keV electrons (a), most are reflected and a bright image is produced on the SEM, while for 7 keV electrons (b), the absorption coefficient is higher and the detecting metal seems darker. The output for 3, 4 and 5 keV electrons, at 1 nA current is shown in (c)-(e)

5. SUMMARY

A front-side bombarded electron detector has been described. The detection is achieved by a metal layer which also serves as a protective layer. We described several implementations of the detector, and described a test chip utilizing the capacitor-type pixel. The test chip was tested for circuit functionality using an electrical model of electron bombardment, and for actual detection inside a SEM. Results indicate correctness of concept, and laboratory measurements are backed up by theoretical calculations. Future research will deal with minimizing metal oxidation, incorporation the detector into an array, and optimizing fast-readout and adaptive architectures for the new detection mechanism.

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