ELSEVIER

Journal of Neuroscience Methods 153 (2006) 21–26

JOURNAL OF NEUROSCIENCE METHODS

www.elsevier.com/locate/jneumeth

Analog frontend for multichannel neuronal recording system with spike and LFP separation

Yevgeny Perelman *, Ran Ginosar

VLSI Systems Research Center, Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa 32000, Israel

Received 31 May 2005; received in revised form 27 September 2005; accepted 30 September 2005

Abstract

A 0.35 μm CMOS integrated circuit for multi-channel neuronal recording with twelve true-differential channels, band separation and digital offset calibration is presented. The measured signal is separated into a low-frequency local field potential and high-frequency spike data. Digitally programmable gains of up to 60 and 80 dB for the local field potential and spike bands are provided. DC offsets are compensated on both bands by means of digitally programmable DACs. Spike band is limited by a second order low-pass filter with digitally programmable cutoff frequency. The IC has been fabricated and tested. 3 μV input referred noise on the spike data band was measured.

Keyword: Multi-channel recording

1. Introduction

Recent advances in fabrication of MEMS microelectrode arrays (Bai et al., 2000; Maynard et al., 1997), together with the ability of coupling the arrays directly to VLSI chips, allow simultaneous monitoring of tens and even hundreds of neurons. Moreover, clinical applications of brain–machine interfaces may require monitoring of much larger populations, even hundreds and thousands of neurons (Nicolelis, 2001).

With this large a number of recording units, communicating raw neuronal signals results in prohibitively large data rates (Harrison, 2003). When sampled with 20 ksps, eight bit precision, even a hundred of electrodes would generate 16 Mbps, too large for common methods of low-power wireless communications. Evidently, some form of data reduction must be applied prior to communication.

It is possible to detect the presence of neuronal spikes as demonstrated by Harrison (2003) and communicate only active portions of recorded signals. Assuming an electrode might "sense" two or three units which fire 20 times per second on average, and taking the firing event length to be 2 ms, only 10 times data rate reduction can be achieved. Further reduction can be provided by restricting the communicated information to mere indications of spike presence.

An extracellular microelectrode typically senses activity from several units adjacent to its tip. Spike sorting (Lewicki, 1998) applies classification techniques to assign spike waveforms of different shapes to different units. With on-chip spike sorting, the data bandwidth is reduced to 200 kbps (almost a hundred times) for the figures above, assuming a 32 bit message generated for every spike.

Another reason for on-chip sorting is brought by Zumsteg et al. (2004). In autonomous motor prosthetics, assuming that every spike coming from a certain electrode is generated by the same unit might prove not sufficiently accurate for movement trajectory calculations. Zumsteg et al. (2004) shows also that implementation of existing algorithms for on chip spike sorting is feasible in terms of power dissipation.

1.1. Motivation of this work

In a signal recorded by an extracellular microelectrode, neuronal firing activity occupies the 100–10.000 Hz frequency band; its amplitude is typically lower than 500 μV. The *Local Field Potential* (LFP) occupies the lower frequencies, below 100 Hz, with amplitudes below 5 mV. The signal-to-noise ratio of the

* Corresponding author.
E-mail addresses: perelman@tx.technion.ac.il (Y. Perelman), ran@ee.technion.ac.il (R. Ginosar).

0165-0270/$ – see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.jneumeth.2005.09.017

combined signal is rather large: as the microelectrode noise (Borkholder, 1998) and background noise of cortical activity (Guillory and Normann, 1999) are typically 5 μV, it may reach 60 dB.

Since the LFP must be filtered out prior to spike sorting, it is possible to block it right at the front-end (Obeid et al., 2003), by high-pass filtering below 100 Hz. It was shown, however, that LFP carries important information (Arieli et al., 1996; Donoghue et al., 1998). Several front-end circuits pass the LFP band intact (Harrison and Charles, 2003; Mohseni and Najafi, 2001; Patterson et al., 2004). They block the large input DC offsets, typical for neuronal signals, by high-pass filtering below 1 Hz. As the entire combined signal is passed, the minimal required precision of subsequent data acquisition is 10 bit, defined by the signal SNR. The maximal gain is limited by the LFP magnitude and chip supply voltage. Since the firing activity (SPK) has ten timer lower magnitude than the LFP, it can be amplified only to one tenth of the output swing.

To overcome these limitations, we suggest splitting the signal into two bands after the first amplification stage. Thus, the LFP and SPK parts can be processed by separate channels, amplifying both to the full swing. Consequently, the system dynamic range needs only be a 100, as determined by the SNR of the SPK signal. Thus, no more than seven bits data acquisition is required: with seven bits A/D conversion of 500 μV signal, the LSB step would be 4.5 μV. The associated quantization noise is $4.5/\sqrt{12} = 1.3\,\mu V$, lower than the 5 μV signal noise.

In this paper we present an integrated CMOS front-end for neuronal recording from implanted electrodes capable of delivering both spike data and the local field potential from twelve true-differential recording channels. The front-end is intended for further integration on a head-stage with an external wireless interface.

Following the overall system architecture along with some basic parameter constraints and the preamp circuit, the paper presents the measurement results of the fabricated test chip.

2. Architecture

A 0.35 μm CMOS twelve-channel neuronal recording front-end IC was designed with true-differential inputs, so that each electrode can be referenced to any point in the system. The amplification channel was designed to have an RMS noise level of 2–3 μV in the band of 0.2–10 kHz.

The block diagram of a single channel is shown in Fig. 1.

The input signal is first cleared of the dc offsets by a single-pole input high-pass filter. The corner frequency should be of several Hertz, in order to pass the LFP part of the signal intact. The resistors (8 MΩ) were placed on-chip, whereas the capacitors must be added externally. The IC was intended to couple to electrodes with 0.1–1 MΩ characteristic impedance (measured at 1 kHz). Since electrode impedance typically exhibits $1/f^{0.5,\ldots,1}$ dependence, 8 MΩ input resistors provide a good impedance mismatch at frequencies of several hundred Hz and above, namely at SPK band. However, the lower part of LFP band may be shunted, especially when used with electrodes of the higher impedance range. Hence, larger resistors should be considered for the future versions of the recording channel.

Stimulation artifacts is another known issue with microelectrode recording. Strong stimulation signals may saturate the recording channel that may potentially take a long time to settle back, even after the stimulation has been de-asserted. The core of this problem does not relate to the amplifying circuitry, which has a (relatively) high bandwidth of at least 10 kHz and will leave saturation within several hundreds of microseconds. The main issue is with the input HPF, that has a very high time constant. Our architecture allows for nulling the input HPF by a digital switch (Fig. 1). A saturation condition can be detected at the output of the amplifiers, nulling the corresponding HPFs. Even with this arrangement, after the nulling switches open, slow discharge of the electrode capacitance may cause slow slewing of the input potential.

The first stage provides an amplification of 40 dB to a single-ended output, which is band-split by a first-order RC filter into

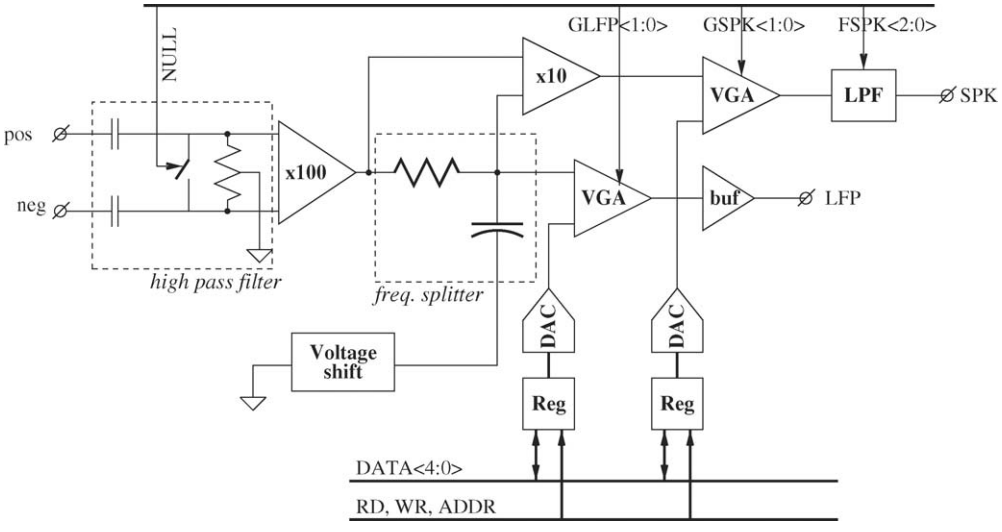

Fig. 1. A single channel block diagram.

high frequency SPK (neuronal firing activity) and low frequency LFP parts. The splitter pole was roughly placed at 200 Hz, by using a 5 MΩ resistor (high-resistive poly) and 160 pF (gate-oxide) capacitor. Ground voltage is shifted up for MOS capacitor bias with a source follower. Variations in poly sheet resistance and gate-oxide thickness can shift the pole between 150 and 250 Hz, as predicted by process corner parameters.

The minimal gain to be provided by the first stage is determined by noise constraints as follows. RMS noise introduced by the resistor into the signal (at room temperature) is:

$$\sqrt{4\,\mathrm{kTR}\,f_0} = 28\,\mu\mathrm{V}$$

assuming the output LPF has a steep roll-off above $f_0 = 10$ kHz. The first stage gain is required to be well above 20 dB in order to keep the input referred noise of the high splitter resistance below 3 μV. First stage gain of 40 dB was taken as a design goal.

The low frequency LFP signal is amplified by a variable-gain amplifier (VGA) and buffered to chip outputs. The VGA provides digitally selectable gains of 2.5/5/7.5/10×. Thus, the maximum total gain of the LFP channel was designed to be 60 dB.

The high frequency SPK signal is amplified by a factor of 10 and by another VGA (to a total maximum of 80 dB). Its upper corner frequency is limited by a second-order Bessel LPF, implemented (for the sake of simplicity) as a continuous time Sallen-Key RC biquad (Deliyannis et al., 1999). Resistors are implemented as serially connected polysilicon segments, which can be selectively shortened by means of a three-bit controlling signal. Filter cutoff can be varied that way in the range of 8.5–13 kHz.

Although successful implementation of a neuronal signal processing channel based on switched capacitor filter has been reported (Obeid et al., 2003), we have decided to design continuous-time analog circuits, to avoid contaminating the input with switching noise. Switched capacitor implementation for filters can provide for better time-constant accuracy and smaller area, neither of which was our main design goal.

DC offsets of both the SPK and LFP channels have to be compensated: LFP channel amplifies the input preamp offset (100 μV, typically) by up to 60 dB; unless compensated, it would limit the dynamic range severely or even saturate the VGA. SPK channel offset is determined by the offset of the 10× stage amplified by 40 dB, as the DC part of the preamp output signal is cut off by the band splitter. Smaller than LFP, preamp offset is yet significant: the 10× stage has larger input offset compared to the preamp, since the latter uses very large input devices due to the noise requirements.

Offset compensation is carried out by two calibration DACs (one for LFP and one for SPK) applied to the last amplification stages (VGAs). The DACs are implemented as five-stage R2R resistor ladders, having 400 mV output swing. DAC values are stored in registers that can be individually accessed by the controller through a common bus with five address/data bits and three control bits. The controller calibrates the outputs, one by one, upon de-assertion of the RST signal (Fig. 2). A very simplistic calibration algorithm is used, identical for both SPK and LFP. First, the highest DAC voltage is selected, setting the calibrated output at the lower rail. Then, the DAC is stepped down by a single LSB step at a time, while the channel output is constantly compared with the mid-point (ground potential). As soon as the channel output crosses the mid-point, the process is stopped and the next channel is calibrated.

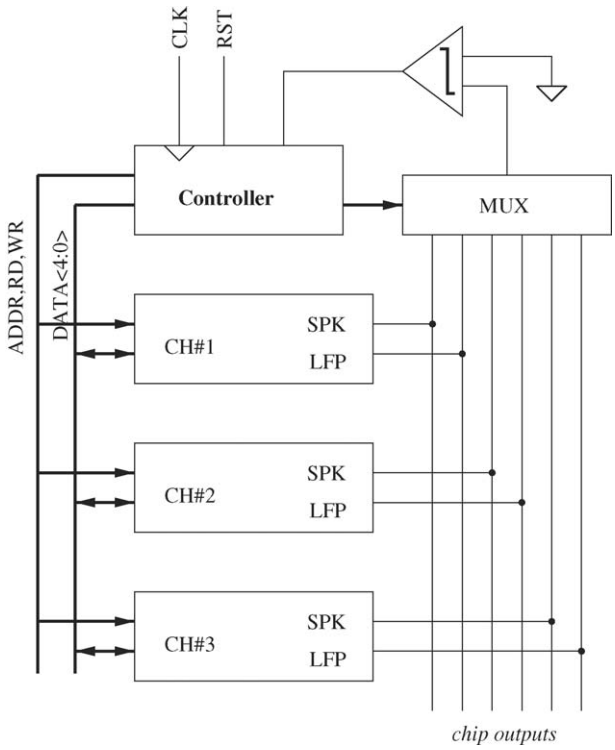

Fig. 2. Chip architecture.

3. Input preamplifier

The input preamplifier must provide a sufficiently high input impedance in order not to overload the high-impedance recording electrode. The noise level requirement is dictated by the inherent noise of the recording electrode and cortical background noise, both of which having magnitude of several microvolts. In addition, the preamp must have a flat frequency response starting from DC and use no switching circuits. A differential circuit addressing the above requirements is shown in Fig. 3.

This is a degenerated differential cascoded transconductor stage, loaded with a resistor to convert the output current back to voltage. The disadvantage of this circuit is the gain error due to the finite transconductance of input transistors. The gain of the circuit in Fig. 3 is given by:

$$A = \frac{2R}{r + r_m} = \frac{2R/r}{1 + r_m/r}$$

where r_m is the transresistance of $M_{1,2}$. While r can be matched to R by using the same resistor types and employing appropriate layout techniques, there is no straightforward way of matching r to r_m. The sensitivity to r_m can be reduced by reducing the ratio r_m/r, but there is a limit on how high r can be due to the noise requirements (some 10 kΩ) and reducing r_m means more power.

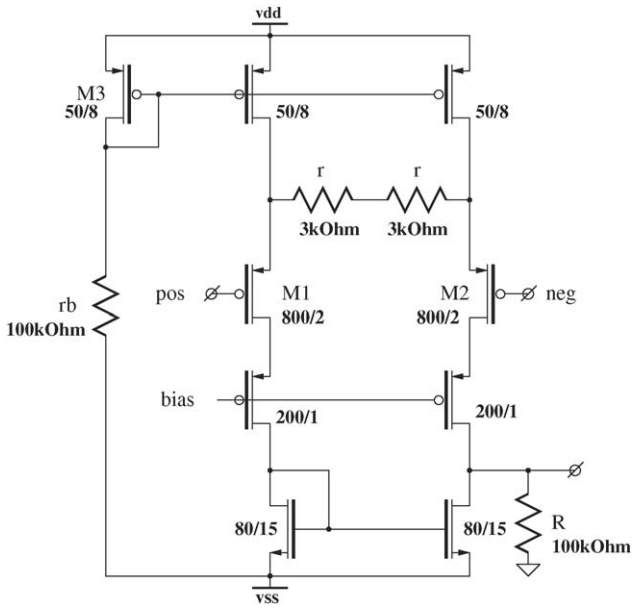

Fig. 3. Input preamplifier circuit topology.

Instead, we match r to r_m by appropriately controlling the bias currents through $M_{1,2}$. $M_{1,2}$ are operated in the subthreshold region (the smallest r_m for a given I_d) so that r_m is inversely proportional to I_d:

$$r_m = \frac{\kappa V_{th}}{I_d}, \qquad V_{th} = \frac{kT}{q}$$

I_d is given by:

$$I_d = \frac{V_{dd} - V_{gs3}}{r_b}$$

thus we can write the gain as:

$$A = \frac{2R}{r + r_b \kappa V_{th}(V_{dd} - V_{gs3})}$$

We match r_b to r and keep V_{gs3} much lower than V_{dd}. Since the ratio of V_{th} and V_{dd} is small, the above expression becomes weakly dependent on process parameter κ, and on V_{gs3}. The chip is expected to work in constant temperatures (subject body), thus the dependence on V_{th} is not worrying. One sigma chip-to-chip channel gain variation of less than 2% was actually measured.

Table 1
Electrical test results summary

SPK gain	77 dB
LFP gain	58 dB
SPK noise (RMS)	3.1 μV
LFP noise (RMS, above 1 Hz)	5 μV
Output offset (highest gain)	Below 50 mV
Channel power	3.3 mW
Output LPF cutoff	8–13 kHz
Band splitter frequency	330 Hz
SPK THD (1 Vpp, 1 kHz sine)	Below 1%
LFP THD (1 Vpp, 0.1 kHz sine)	Below 1%

4. Measurement results

The chip was fabricated using AMS 0.35 μm quad-metal, double poly CMOS process with 3.3 V power supply (Fig. 4). Ten fabricated chips were tested electrically. Input signals were produced by a function generator, with successive −60 dB amplitude reduction to achieve microvolt levels. Noise was measured with grounded inputs. Input noise currents are not expected to affect the noise floor: since the circuit uses MOS devices, there is only negligible current flow into the gates. The only sources of input current noise are the ESD protection structures inside the IC bond pads. The leakage currents of the pad structures are estimated below 10 pA. The associated RMS shot noise over 10 kHz bandwidth with 1 MΩ input impedance is 140 nV, far below the preamplifier noise floor.

Some of the electrical test results are summarized in Table 1. While most of the design goals were met, note that band splitter frequency is somewhat displaced. This is due to a failure in the band-splitter MOS capacitor biasing circuit. Too low a bias voltage has placed the MOS capacitor at the steep region of the C–V curve: the gate capacitance is therefore much lower than expected and it exhibits high variations. This results in a misplaced band splitter corner frequency and in significant variations of that frequency, both are clearly seen in Fig. 5.

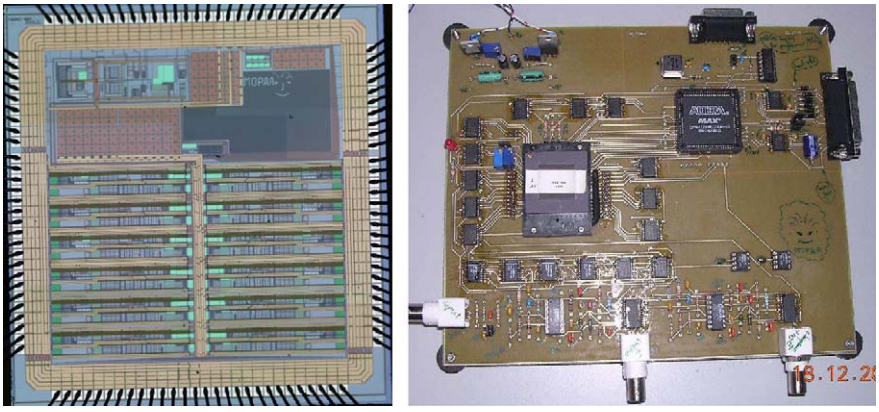

Fig. 4. Chip micrograph and test board.

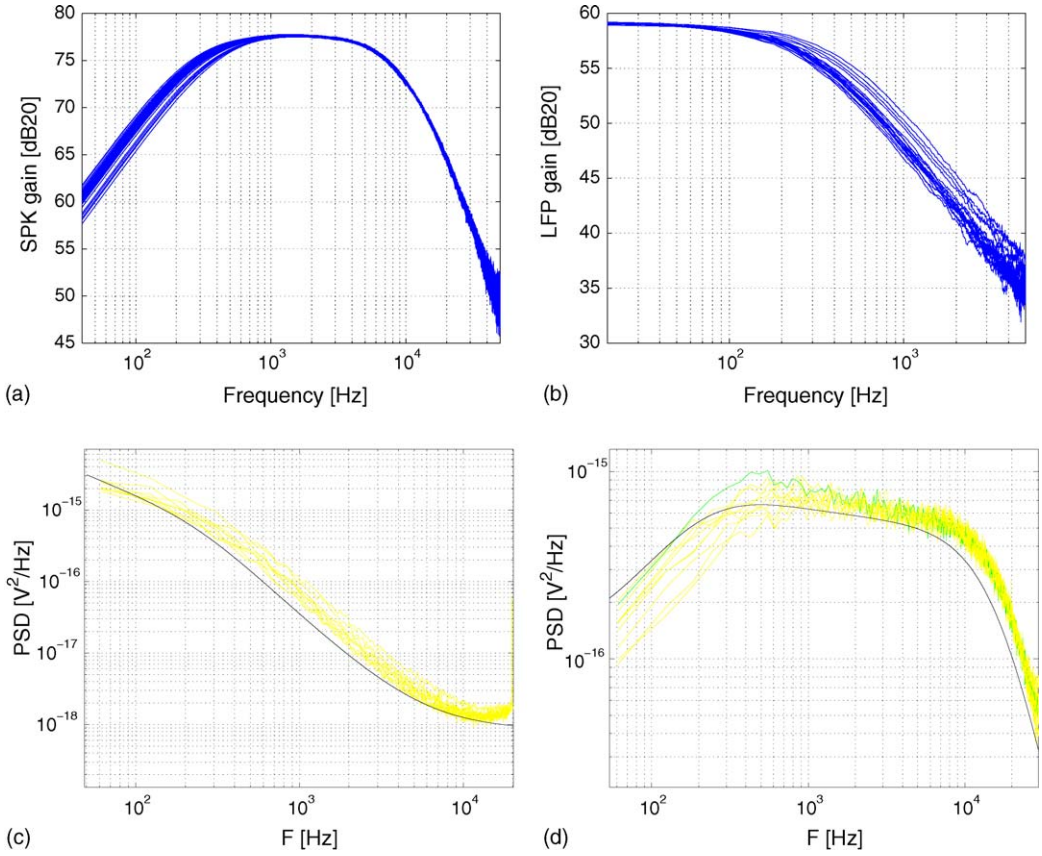

Fig. 5. Cumulative plots: (a) and (b) spike and LFP frequency response; (c) and (d) spike and LFP output noise PSD, divided by respective gains.

The measured magnitude of frequency response for SPK and LFP bands is shown in Fig. 5(a) and (b). The frequency response is quite stable over all the measured chips. Fig. 5(c) and (d) shows the spectral densities of SPK and LFP output noise for several measured chips, divided by SPK and LFP gains, accordingly. Solid lines denote simulated curves. *I/f* noise dominates over the LFP band and thermal noise dominates over the higher frequency SPK band. Power dissipation of 3.3 mW per channel was measured.

Fig. 6 shows measurement of SPK channel gain and LPF cutoff frequency for various settings of the respective controls. The control of the latter determines how many serial resistor segments are connected inside the LPF, thus the control value is directly proportional to the time constant and inversely proportional to frequency.

Fig. 7 presents an in vivo recording segment, recorded using a Michigan probe (Vetter et al., 2004) implanted into rat cortex.

5. Summary and discussion

A low noise, dual band, twelve channel differential front-end IC for neuronal recording has been implemented in 0.35 μm CMOS technology. The front-end provides for a complete recording channel with a preamplifier, digitally controlled vari-

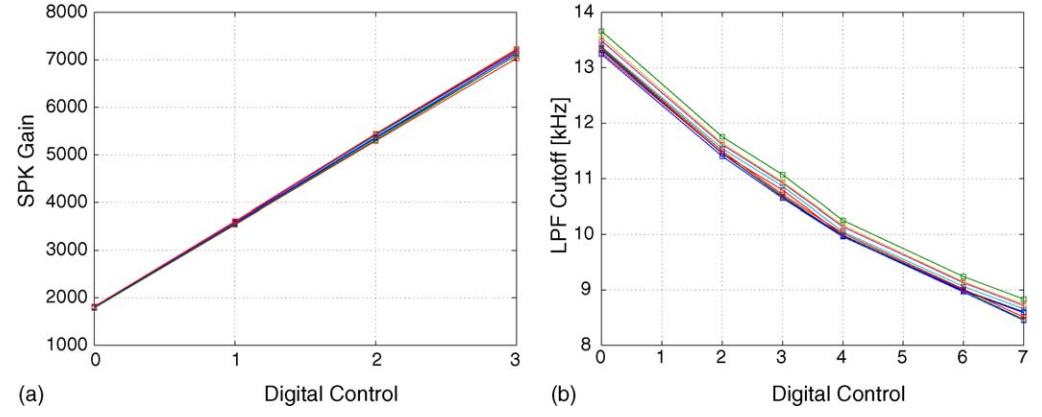

Fig. 6. Cumulative plots: (a) SPK gains for vs. digital control setting; (b) LPF cutoff frequency vs. digital control setting.

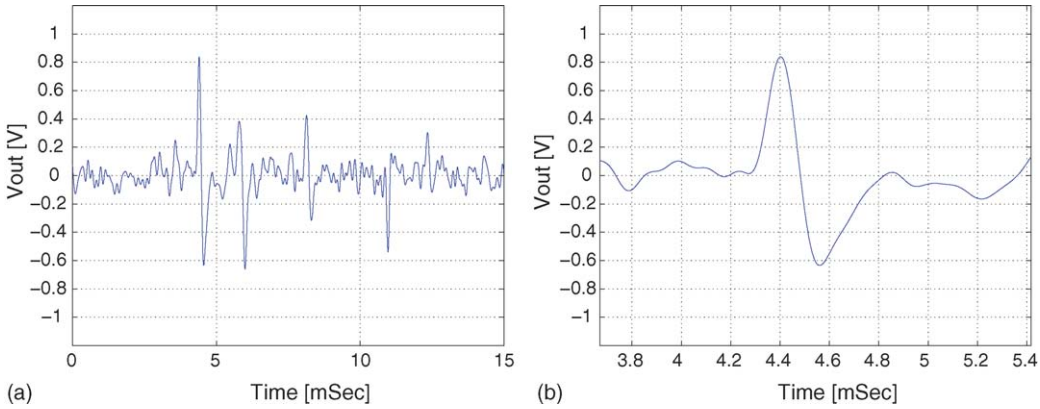

Fig. 7. In vivo measurement: (a) signal segment; (b) close up on a large spike.

able gain output amplifiers, output low-pass filter with digitally controlled cutoff frequency and digital offset compensation. Band-splitting the recorded signal into spike (high-frequency firing activity) and LFP (low-frequency local field potential) bands allows for significant reduction of the output dynamic range with subsequent reduction in required data acquisition precision. Digitally calibrated offset compensation at LFP and SPK channels and 2–3 stage amplification enable 60 and 80 dB gains, respectively.

Measurements demonstrate that gain and noise requirements were met. Power consumption was measured at about 3.3 mW per channel.

Current research addresses the issues of power dissipation, on-chip integration of the input HPF and A/D conversion. Power dissipation can be reduced by employing active filters (such as g_m/C) and by proper scaling of the later amplification stages to operate on lower currents, as the noise requirements on those stages are relaxed.

References

Arieli A, Sterkin A, Grinvald A, Aertsen A. Dynamics of ongoing activity: explanation of the large variability in evoked cortical responses. Science 1996;273:1868–71.

Bai Q, Wise KD, Anderson DJ. A high-yield microassembly structure for three-dimensional microelectrode arrays. IEEE Trans Biomed Eng 2000;47(3):281–9.

Borkholder DA. Cell based biosensors using microelectrodes. Ph.D. Thesis, University of Stanford, 1998.

Deliyannis TL, Sun Y, Fidler JK. Continuous-time active filter design. CRC Press; 1999.

Donoghue JP, Sanes JN, Hatsopoulos NG, Gaal G. Neural discharge and local field potential oscillations in primate motor cortex during voluntary movements. J Neurophysiol 1998;79(1):159–73.

Guillory K, Normann R. A 100-channel system for real time detection and storage of extracellular spike waveforms. J Neurosci Meth 1999;91:21–9.

Harrison RR. A low-power integrated circuit for adaptive detection of action potentials in noisy signals. In: Proceedings of the 25th IEEE EMBS ann. international conference; 2003. p. 3325–8.

Harrison RR, Charles C. A low-power low-noise cmos amplifier for neural recording applications. IEEE JSSC 2003;38(6):958–65.

Lewicki MS. A review of methods for spike sorting: the detection and classification of neural action potentials. Network 1998;9(4):R53–78.

Maynard EM, Nordhausen CT, Normann R. The utah intracortical electrode array: a recording structure for potential brain-computer interfaces. Electroencephalogr Clin Neurophysiol 1997;102:228–39.

Mohseni P, Najafi K. A fully integrated neural recording amplifier with dc input stabilization. IEEE Trans Biomed Eng 2001;51:5.

Nicolelis M. Actions from thoughts. Nature 2001;409:403–7.

Obeid IC, Morizio JKA, Moxon MALN, Wolf PD. Two multichannel integrated circuits for neural recording and signal processing. IEEE Trans Biomed Eng 2003;50(2):255–8.

Patterson WR, Song YK, Bull CW, Ozden I, Deangellis AP, Lay C, et al. A microelectrode/microelectronic hybrid device for brain implantable neuroprosthesis applications. IEEE Trans Biomed Eng 2004;51:10.

Vetter R, Williams J, Hetke J, Nunamaker E, Kipke D. Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex. IEEE Trans Biomed Eng 2004;51(6):896–904.

Zumsteg ZS, Ahmed RE, Santhanam G, Shenoy KV, Meng TH. Power feasibility of implantable digital spike-sorting circuits for neural prosthetic systems. In: Proceedings of the 26th IEEE EMBS Ann. International Conference; 2004. p. 4237–40.