Symmetric Boost Synchronizer for Robust Low Voltage, Low Temperature Operation

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Abstract

Modern Systems-On-Chip (SoC) contain multiple asynchronous clocks and the various modules exchange signals and data across the clock domains. These signals are often subject to the effects of metastability. Therefore, there is a necessity to synchronize data transfers between clock domains and, as a result, synchronizers are an essential part of any SoC design. Normal synchronizers may fail under extreme conditions of low temperature (such as the outdoors in northern countries at winter nights) and low supply voltage (e.g. when operating on low battery), because both gate delay and the metastability resolution time constant Tau significantly increase under these conditions. We investigate these issues and propose using the boost synchronizer, which achieves Tau of 144ps at V_{DD}=0.35V, T=–20°C in a 70nm CMOS technology while the normal latch incurs Tau of 1,332ps under the same conditions.

1. Introduction

Modern system-on-chip (SoC) designs typically contain many separate clock domains. Clock-domain crossing signals are often subject to the effects of metastability, and hence they must be synchronized by the receiver circuit. Normal synchronizers, such as those employing two flip-flops [1], have been found to fail under extreme conditions of low temperature (such as the outdoors in northern countries at winter nights) and low supply voltage [2]. The latter problem is important in the case of mobile, battery operated devices that need to operate as long as possible on a diminishing battery charge. Very few synchronization circuits have been developed to mitigate the problem of low supply voltage (e.g. [3]), and none so far have been proposed for solving both problems simultaneously.

In this paper we present a *symmetric boost latch* that is capable of synchronizing reliably in conditions of low supply voltage and low temperature. The key property of the symmetric boost latch is the ability to dynamically change its transconductance. This is achieved by employing a pair of pull-up transistors which inject current into the cross-coupled inverters that form the latch. As a result of current injection the transconductance (g_m) of the transistors increases and this leads to faster resolution of metastability. The principle of the symmetric boost latch has been inspired by the synchronizers presented in [3], [4], [5]. Similar study has been presented in [6].

The symmetric boost latch was designed using BPTM 70nm process transistors [7][8] and simulated with SpectreS. The simulation circuit is based on the method described

in [9] to determine τ, the exponential metastability resolution time constant. A somewhat similar method has been presented in [10]. The simulations show notable improvement in τ, especially in conditions of low supply voltage and low temperature, and as a result a significant enhancement of MTBF.

The paper is organized as follows: synchronization terms and simulation are described in Section 2. The effects of low temperature and low supply voltage on delay and synchronization are explained in Section 3, and the symmetric boost latch is presented in Section 4, including its theoretical analysis and simulations.

2. Synchronization

Usually, a flip-flop (Figure 1) is used as a basic synchronizer. The flip-flop may become metastable when the setup or hold time of the flip-flop is violated and as a result normal operation is disturbed. Metastability occurs in any system where the data can change randomly with respect to the system clock, e.g. in any GALS (Globally-Asynchronous Locally-Synchronous) design. If the flip-flop or latch is metastable, its propagation delay might lengthen or it could get trapped in a logically undefined intermediate voltage level for an indefinite length of time.

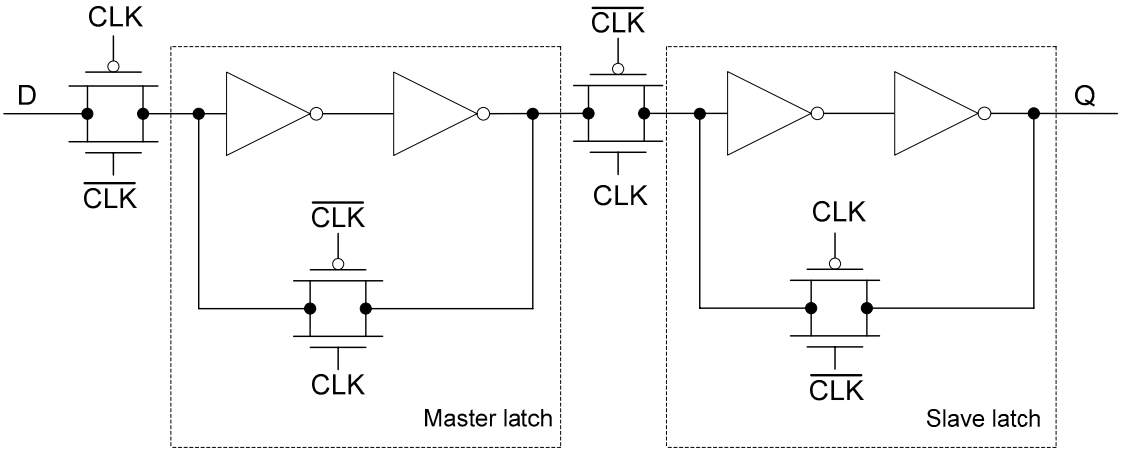

Figure 1 Typical Edge Triggered D Flip-Flop

After the sampling (rising) edge of the clock the master latch is opaque, and the slave latch is transparent. If the flip-flop is metastable, only the master latch is metastable. Hence the efforts to mitigate the metastability problem focus on the master latch.

A synchronizer is characterized by three principal parameters:

- τ, the resolution time constant.
- T_W, the metastability window, related to the setup/hold window of a flip-flop [9][10].
- MTBF, the Mean Time Between Failures.

The resolution time constant τ of a synchronizer can typically be expressed as [11]:

$$\tau = \frac{C}{g_m} \tag{1}$$

where g_m is the synchronizer transconductance, and C is capacitance. The metastability window T_W can be estimated at about 2–4 FO4 gate delays [1][2]. The MTBF is given by:

$$\mathrm{MTBF} = \frac{e^{S/\tau}}{T_W f_C f_D} \tag{2}$$

where S is the time allocated for settling, f_C is the clock frequency and f_D is the data arrival rate.

Certain parameters are optimized in order to enhance MTBF. Usually, the parameters f_D and f_C cannot be changed (they represent the performance targets of the system). Therefore, most design efforts are concentrated on reducing the metastability window T_W, and reducing the resolution time constant τ. Reducing τ is more significant, since the MTBF exhibits exponential dependence on this parameter, while dependence on T_W is only linear. As shown above, τ depends mostly on g_m and C of the first latch in the synchronizer. This paper focuses on reducing the resolution time constant.

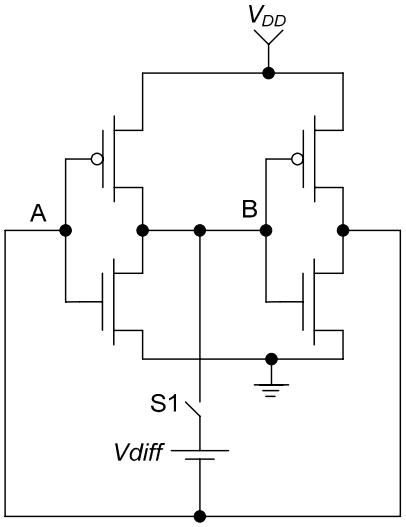

Figure 2 Typical metastability simulation circuit

A metastability simulation circuit is shown in Figure 2 [9]. The circuit is used mostly to determine τ. All transistors have the same size, as suggested in [12], and their W/L ratio is 70nm/70nm. The threshold voltage of the transistors is ~0.2V.

Initially, nodes A and B are shorted together by the switch S1, forcing the latch into a metastable state. The cross-coupled inverters have the same size, and hence their thresholds are (ideally) identical. At some time t_0 the switch is opened, allowing the nodes to drift apart, one node to V_{DD} and the other one to ground. The switch opening simulates the sampling edge of the clock. Battery *Vdiff* is placed across the nodes to ensure the starting time and to enable control over the direction of divergence. Typical simulation results are presented in Figure 3 and Figure 4. The chart in Figure 3 shows the voltage of the diverging nodes, and Figure 4 shows the logarithm of the voltage

difference of the two nodes. The inverse of the slope of the line in Figure 4 defines τ, which can be calculated by [9]:

$$\tau = \frac{t_2 - t_1}{\ln(V_2 / V_1)} \tag{3}$$

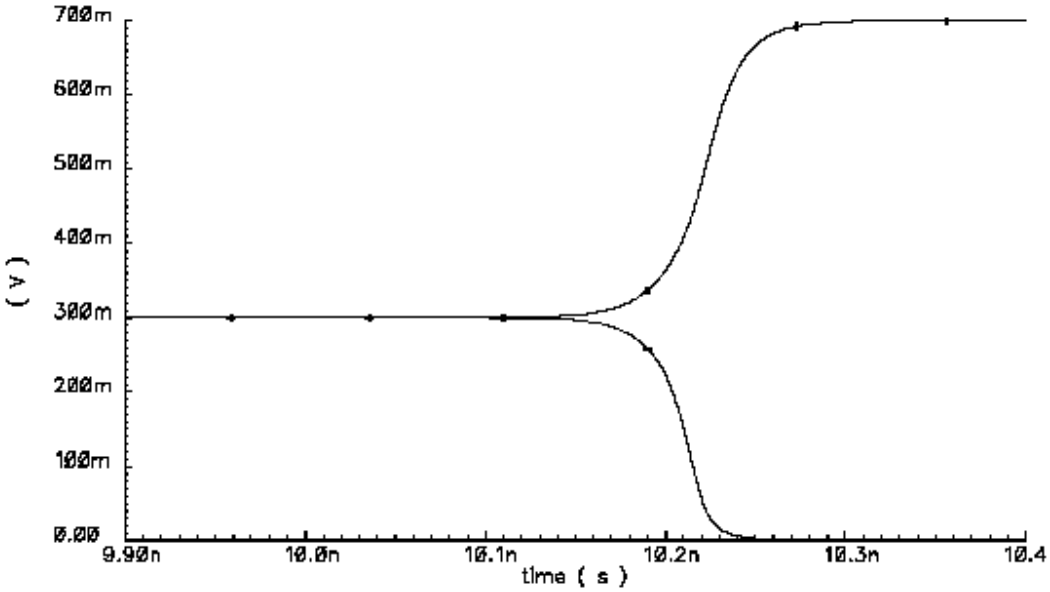

Figure 3 Voltage waveform of the diverging nodes of the latch

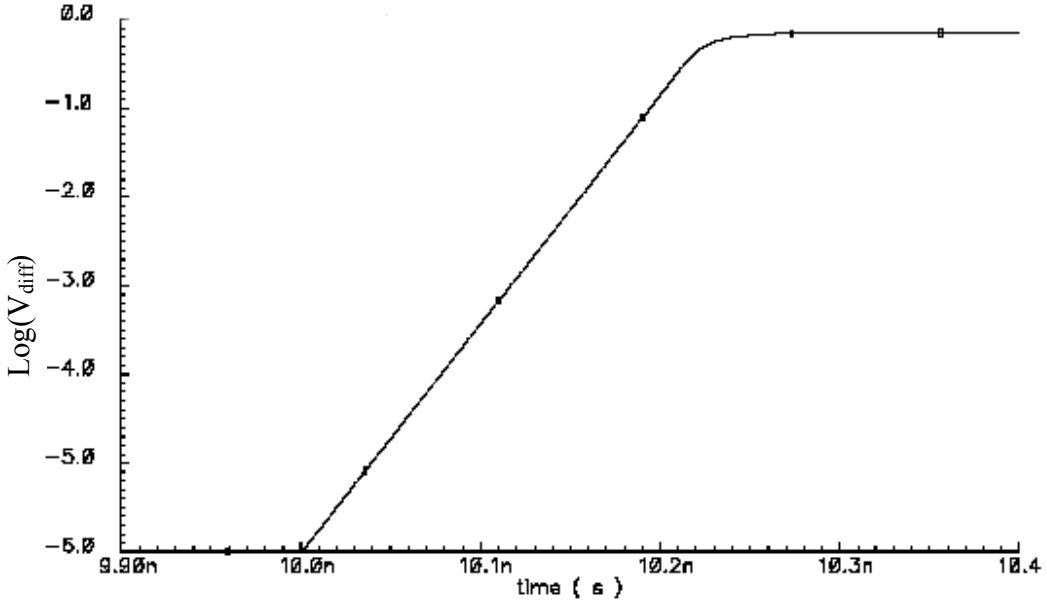

Figure 4 Logarithmic voltage difference. τ is the inverse of the slope of the straight segment

The straight line on the semi-logarithmic chart in Figure 4 implies that the resolution behaves exponentially.

3. Temperature and supply voltage effects on synchronization

The delay of a CMOS device operating in the saturation region is inversely proportional to the drain current [13]:

$$\text{Delay} \propto \frac{CV_{DD}}{I_D} \propto \frac{CV_{DD}}{(V_{DD} - V_{th})^{\alpha}} \tag{4}$$

Where:

I_D - drain current,
V_{th} - threshold voltage,
α - velocity saturation index, typically around 1.3.

The resolution time constant τ is inversely proportional to the synchronizer transconductance, g_m (Eq. (1)). When the transistor is in saturation, the transconductance is proportional to the square root of the drain current I_D ([14] Eq. 2.18):

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{5}$$

Thus, when the synchronizer operates at low supply voltage conditions, the decrease of the drain current I_D both lengthens the delay and extends the time constant τ, since the drain current I_D depends positively on V_{DD} (Eq. (4)).

The drain current is not constant over a wide temperature range. It depends on temperature, and that dependence changes as a function of the supply voltage [15], as shown in Figure 5. When the device is biased near the *zero-temperature coefficient* (ZTC) point, its temperature dependence is minimized. The ZTC point is determined by the characteristics of the MOS devices and the details of circuit layout.

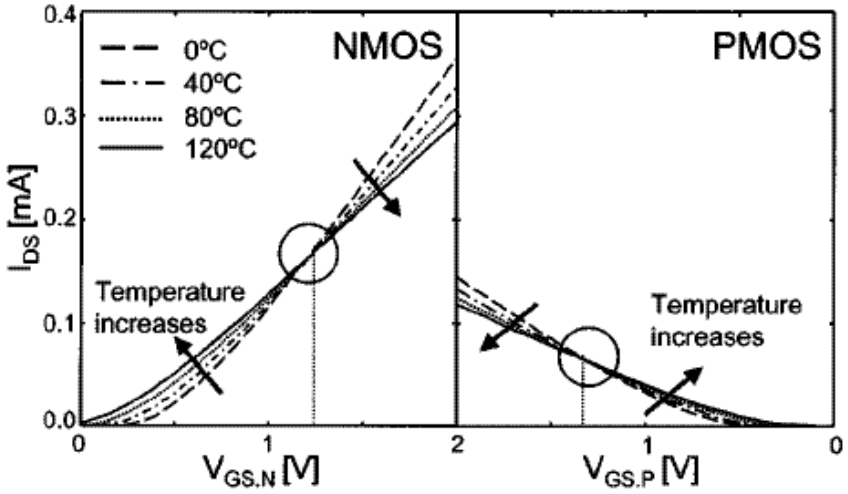

Figure 5 Measured temperature dependence for NMOS and PMOS transistors, temperature range from 0 to 120° C (adapted from [13])

Carrier mobility and threshold voltage exert opposite effects on the drain current. Both carrier mobility and threshold voltage increase when the temperature decreases [16].

Higher mobility increases the current, but higher threshold voltage causes the current to decrease. The overall drain current depends on which of these two processes dominate at a given temperature and supply voltage. At a high supply voltage (V_{DD} higher than the ZTC point and $V_{DD}>>V_{th}$) the drain current is dominantly controlled by the carrier mobility and hence it decreases when the temperature rises. However, when V_{DD} approaches V_{th}, i.e. V_{DD} is lower than the ZTC, the shift in threshold voltage with temperature has stronger effect on the drain current, and as a result the current grows when the temperature rises [16]. More formally, this could be described as follows. The MOSFET drain current I_D in the saturation region ($V_{GS}>V_{th}$ and $V_{GS}-V_{th}<V_{DS}$) is expressed as [13]:

$$I_D \propto \mu(T)(V_{DD} - V_{th}(T))^{\alpha} \tag{6}$$

The threshold voltage $V_{th}(T)$ and the carrier mobility $\mu(T)$ are temperature dependent:

$$V_{th}(T) = V_{th}(T_0) - k(T - T_0) \tag{7}$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{8}$$

where

T	- temperature;
T_0	- room temperature;
k	- threshold voltage temperature coefficient, typically 2.5 mV/K;
m	- mobility temperature exponent, typically 1.5 [13].

Another possible operation mode takes place in the sub-threshold region. When a MOS transistor operates at sub-threshold ($V_{GS}<V_{th}$), its channel is weakly inverted. The drain current I_D exhibits exponential dependence on V_{GS} ([14] eq. 2.30):

$$I_D = I_0 \exp\frac{V_{GS}}{\zeta U_T} \tag{9}$$

where I_0 is a process-dependent constant, $\zeta > 1$ is a nonlinearity factor and $U_T = kt/q$. The transconductance g_m is ([14] Sec. 2.3):

$$g_m = \frac{I_D}{\zeta U_T} \tag{10}$$

I_D decreases exponentially with any decrease in $V_{GS.}$ The decrease in drain current leads to a significant drop of g_m, despite the fact that it exhibits linear dependence on the drain current, rather than square root dependence, as in strong inversion (i.e. when $V_{GS}>V_{th}$, or $V_{DD}>2\times V_{th}$).

As a result of the processes described above, the delay of a logic gate operating at low supply voltage (but not in sub-threshold region) increases as the ambient temperature decreases (in contrast with “normal” behavior). An example of such behavior is shown

in Figure 6. As one can see, at extremely low supply voltage, e.g. about 0.4V (about $2 \times V_{th}$ in the 70nm BPTM process), the gate delay is very sensitive to temperature, and significantly degrades as the temperature decreases. On the other hand, at higher supply voltages the delay decreases when the temperature falls.

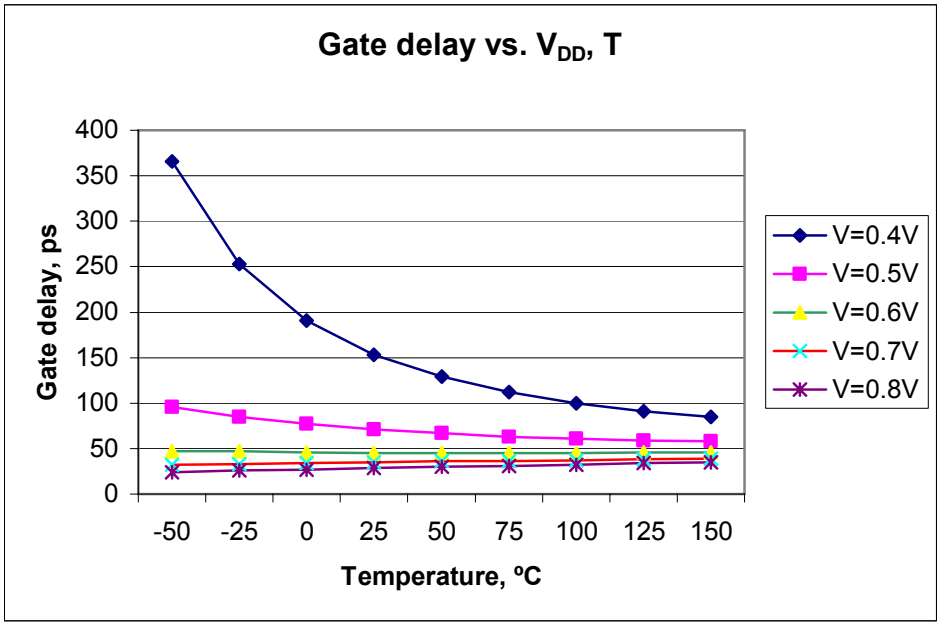

Figure 6 Gate delay vs. V_{DD}, T

As expected, τ significantly increases at low temperature and low supply voltage, since τ depends inversely on either the drain current or its square root. A typical latch was simulated (Figure 2) at different temperatures and supply voltage values and the results are presented in Figure 7.

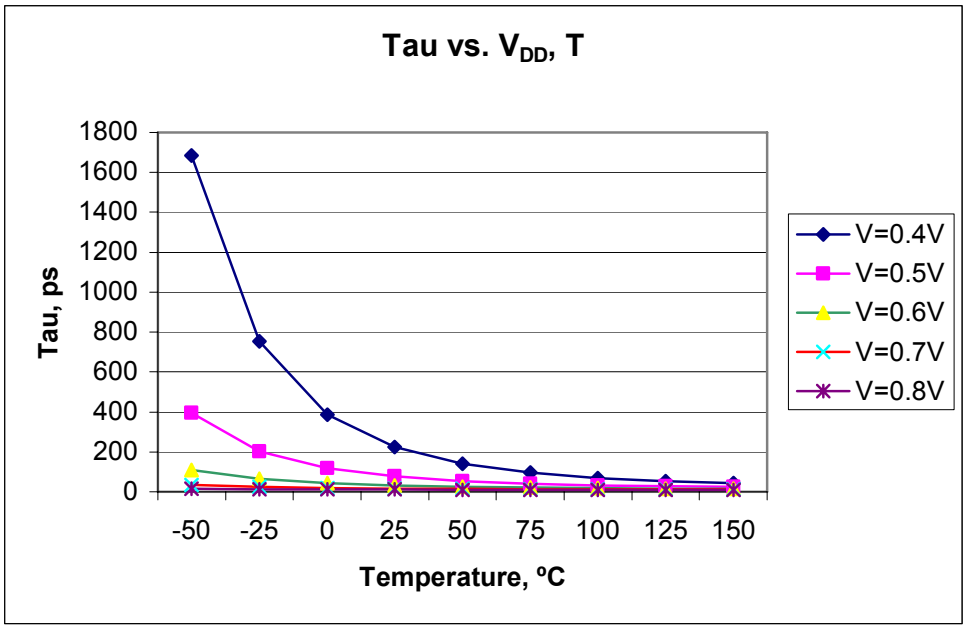

Figure 7 τ dependence on V_{DD}, T

The simulation results demonstrate that metastability becomes a more severe problem at low V_{DD} and low temperature, since both the time constant of a synchronizer and the metastability window lengthen, and the MTBF, which depends on them, gets worse at this condition. In this paper we show how that challenge may be overcome.

The charts in Figure 8 demonstrate the problem. MTBF was calculated according to Eq. (2) for different frequencies, temperatures and supply voltage levels. The settling time S is assumed to be one clock cycle, $f_C=10f_D$ and the metastability window T_W is estimated at 2 FO4 gate delays.

As can be seen in Figure 8, there are three types of response: MTBF rising with temperature showing a concave chart, MTBF rising with temperature but with a convex chart, and MTBF falling with temperature:

1. When the supply voltage is low (0.35V-0.5V), MTBF increases with temperature, and the rate also grows.
2. At medium supply voltage levels (0.6V-0.7V), MTBF grows at a decreasing rate with temperature.
3. At high supply voltage (above 0.9V), MTBF decreases with temperature. At the transition point (0.9V), MTBF initially increases and then decreases.

In summary, MTBF dependence on temperature and supply voltage is quite tricky, and simplistic extrapolations may not apply.

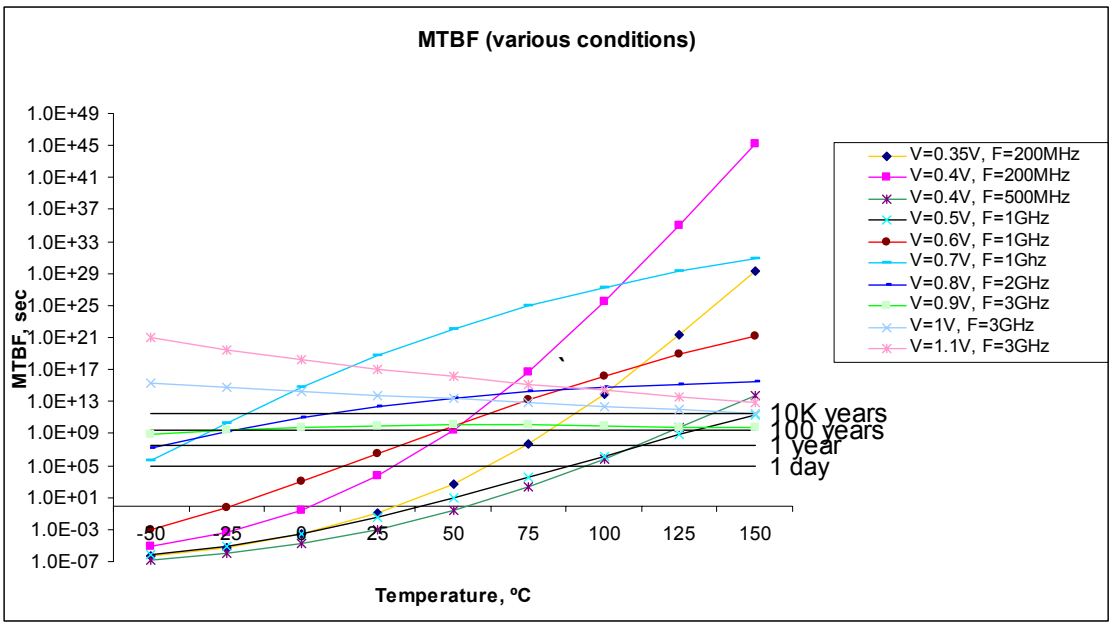

Figure 8 MTBF in various conditions

4. The Symmetric Boost Synchronizer

The symmetric boost latch demonstrates improved performance over the normal latch at low supply voltage and low temperature. A schematic diagram is shown in Figure 9.

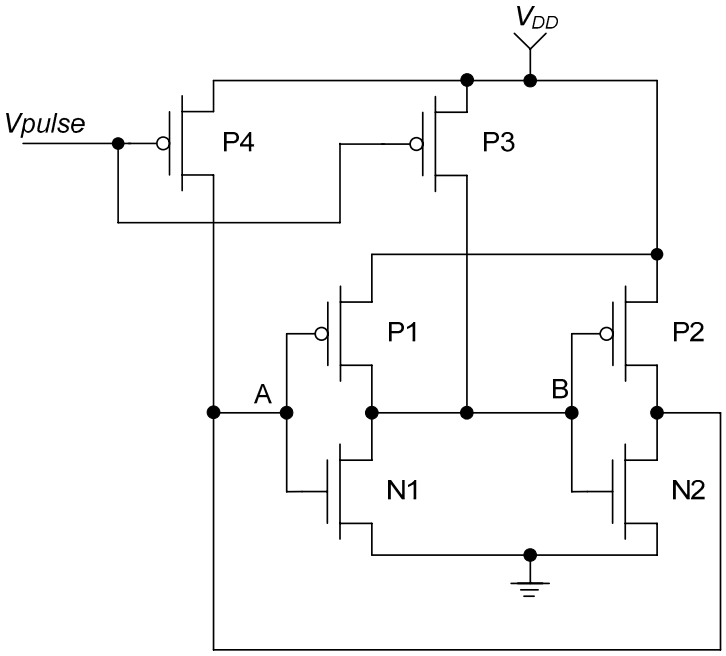

Figure 9 Symmetric boost latch

The latch comprises two cross-coupled inverters (transistors N1, P1, N2, P2) and two pull-up transistors (P3, P4). The purpose of the pull-up transistors is to "boost" the latch when applying a negative pulse to the gates of P3, P4. If the latch is metastable, such a

"boost" accelerates the resolution into one of the two stable states. The negative pulse at the gates of P3, P4 is applied unconditionally, at a delay Δ after the rising (sampling) edge of the clock (Δ could also be zero or even negative). In normal operation, i.e., without any timing violation, the latch is unaffected by the pulse. The choice of the W/L ratio of transistors P3, P4 is based on the following factors, and we found that 150/70 nm works acceptably with minimal size (70/70) inverter transistors:

a) Too weak pull-up transistors may be ineffective "boosters", i.e., if the latch is metastable, it will not resolve quickly enough.
b) Too wide transistors may overload the A,B nodes of the latch with extra capacitance, and as a result slow down latch operation.

The duration of the pulse has to be long enough to allow the latch to become stable after recovering from metastability. It should also not be too long, to reduce power dissipation.

The boost latch has been inspired by the Cline latch [3][4]. Unlike the Cline latch, no additional logic loads the latch nodes, helping to reduce τ, and the pulse may be applied earlier, contributing to faster resolution. A similar approach was employed in [6]. Their improved Jamb latch synchronizer might be superior to the symmetric boost synchronizer in terms of power consumption, since the additional circuitry conducts current only when the latch changes its state and when it is metastable. However, the symmetric boost synchronizer may potentially outperform the improved Jamb latch in terms of τ and T_W, since its nodes are less loaded, and the pulse may be applied earlier, just as in comparison to the Cline latch.

In the rest of this section we first analyze the circuit theoretically and then demonstrate simulation results.

4.1. Theoretical analysis

The analysis of the synchronizer in Figure 9 is based on the following simplifying assumptions [11]:

- The inverters are identical.
- Metastability is defined as the state in which $|V_A - V_B|<V_n$ for some very small noise voltage V_n.
- $V_{thN} = -V_{thP} = V_{th}$.

When the latch is metastable, its operation is affected mostly by thermal noise. This situation continues until the noise makes $|V_A - V_B|$ sufficiently large to "trigger" exponential resolution of the latch.

Assume that $V_{DD}\approx 2V_{th}$ and the latch is metastable, namely $V_A\approx V_B$. The exact level of $V_A\approx V_B$ is determined by the relative on-resistance of N1, N2 and P1, P2, but it is close to $V_{DD}/2\approx V_{th}$. After applying the negative pulse to the gates of P3, P4, A and B nodes are pulled up. Since now P3, P4 pull up in parallel with P1, P2, the new voltage of nodes A, B is higher than before the pulse. Thus, transistors N1, N2 are in saturation ($V_{GS}=V_{DS}$), P1, P2 are in cut-off ($|V_{GS}|<V_{th}$), and P3, P4 are in the ohmic region ($|V_{GS}|-V_{th}>|V_{DS}|$). Actually, transistors P3 and P4 act like non-ideal current sources. Each

inverter is modeled in Figure 10 as a current source pulling current from the pull-up resistor and from the gate oxide capacitance of the two transistors of the other inverter (Figure 10) [11][17].

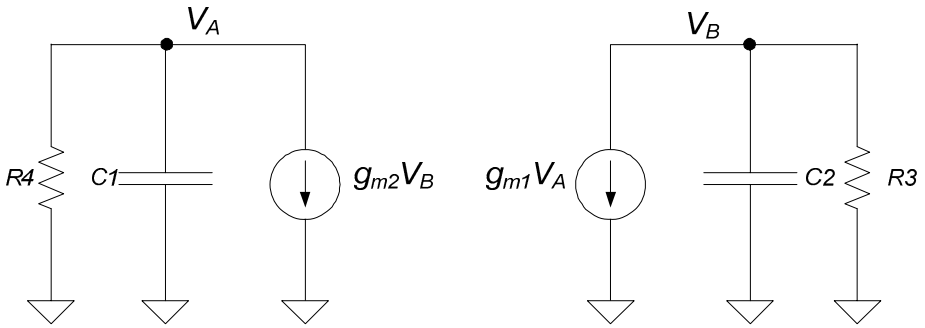

Figure 10 Basic model of the Symmetric boost latch

The small signal model is formulated as follows:

$$\begin{cases} C_1 s V_A + \dfrac{V_A}{R_4} = -g_m V_B \\ C_2 s V_B + \dfrac{V_B}{R_3} = -g_m V_A \end{cases} \tag{11}$$

R3, R4 are the on-resistances of P3, P4 respectively. Let's define $V \equiv V_A - V_B$ and assume that the two inverters are identical, namely C_1=C_2=C, R_3=R_4=R=1/G and $g_{m1} = g_{m2} = g_m$, then

$$sCV = g_m V - V/R = (g_m - G)V \Rightarrow \tag{12}$$

$$sV = \frac{(g_m - G)}{C} V \tag{13}$$

We define:

$$\omega_0 = \frac{1}{\tau_0} \equiv \frac{(g_m - G)}{C} \tag{14}$$

and obtain:

$$sV = \omega_0 V \tag{15}$$

or, in the time domain:

$$\frac{dv(t)}{dt} = \omega_0 v(t) \tag{16}$$

$$\frac{d\ln(v)}{dt} = \omega_0 \tag{17}$$

$$\ln(v) = \omega_0 t + A \tag{18}$$

$$v(t) = Ae^{\omega_0 t} = Ae^{t/\tau_0} \tag{19}$$

The two nodes A, B are also coupled through the various gate-drain capacitances, which could be lumped into a single C_X (Figure 11).

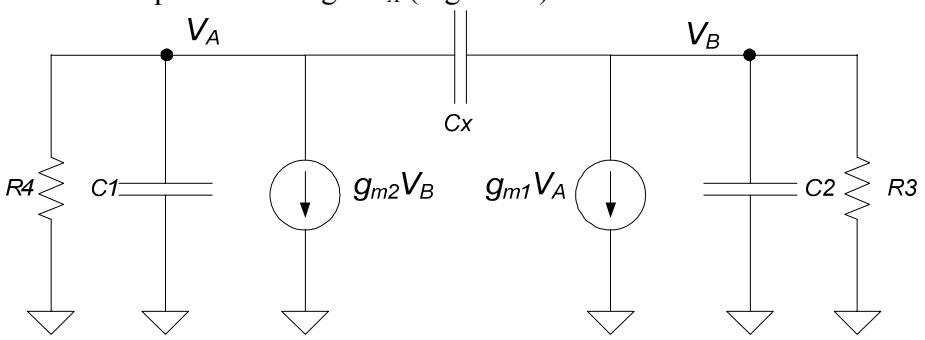

Figure 11 Basic model of the symmetric boost latch with gate-drain capacitance

The expressions for V thus change as follows:

$$\begin{cases} sCV_B + g_m V_A + \dfrac{V_B}{R} + (V_B - V_A)sC_X = 0 \\ sCV_A + g_m V_B + \dfrac{V_A}{R} + (V_A - V_B)sC_X = 0 \end{cases} \tag{20}$$

$$\Rightarrow sC(V_A - V_B) + g_m(V_B - V_A) + \frac{V_A - V_B}{R} + 2(V_A - V_B)sC_X = 0 \tag{21}$$

$$\Rightarrow sCV - g_m V + GV + 2sC_X V = 0 \tag{22}$$

$$\Rightarrow sV(C + 2C_X) = (g_m - G)V \tag{23}$$

$$\Rightarrow v(t) = Ae^{\frac{g_m - G}{C + 2C_X}t} = Ae^{t/\tau} \tag{24}$$

A is determined by the initial conditions and

$$\tau = (C + 2C_X)/(g_m - G) \tag{25}$$

Although the pull-up transistors introduce additional load at the latch nodes (the term -G in the denominator of Eq. (25)), the latch transconductance (g_m) is noticeably higher than that of the normal latch, and the end result is that τ is significantly lower. The

transconductance is proportional to the square root of the bias current I_D (Eq. (5)). The pull-up transistors that act like current sources cause the bias current through transistors N1 and N2 to increase, and this leads to a higher value of g_m. The following figure shows the current through transistor N1, both in the normal latch and in the symmetric boost latch. The circuit was simulated at V_{DD}=0.4V, *Vdiff*=–1μV, and temperature 27ºC.

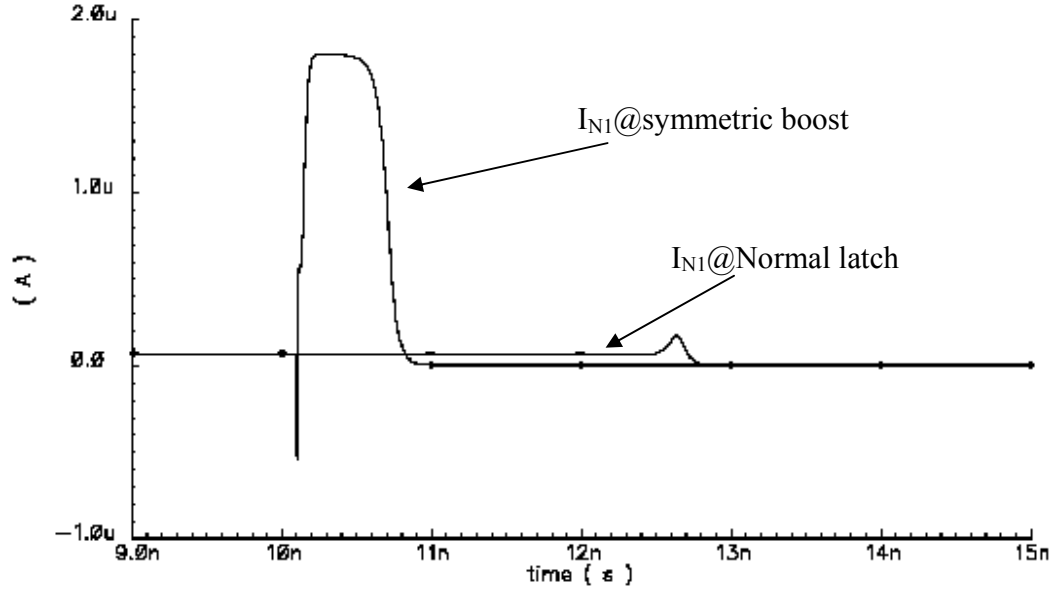

Figure 12 The bias current

As one can see, after applying the pulse at 10.1ns, the bias current in the symmetric boost latch is about 25 times the current through the normal latch (1.8μA vs. 71nA, respectively). This current difference explains why the symmetric boost latch outperforms the normal latch in terms of τ, especially at low supply voltage, although the pull-up transistors introduce extra load at the latch nodes. More simulation results are presented in Section 4.2.

At high V_{DD} the current gain due to the boost transistors is minor relative to the overall latch current. Thus the additional load introduced by these transistors becomes more significant. The simulations show that the extra current and the extra load almost cancel each other, and the time constants of the symmetric boost latch and the normal latch are nearly the same.

Although the symmetric boost is not that effective for operation at high V_{DD}, it is potentially more useful for low V_{DD} operation, when the current gain is more significant than the extra load. It is even more significant at low temperatures, when the effects described in Section 3 severely deteriorate the operation of the normal latch.

4.2. Simulations

The simulation circuit of the symmetric boost latch is shown in Figure 13. First, consider the simulations at temperature 27 ºC and *Vdiff*=-1μV. Switch S1 is opened at t_0=10ns and the pulse of 5ns is applied at t_1= 10.1ns. Since the pulse is longer than the

resolution time, it is effectively equivalent to a step. Figure 14 and Figure 15 show results at V_{DD}=0.7V.

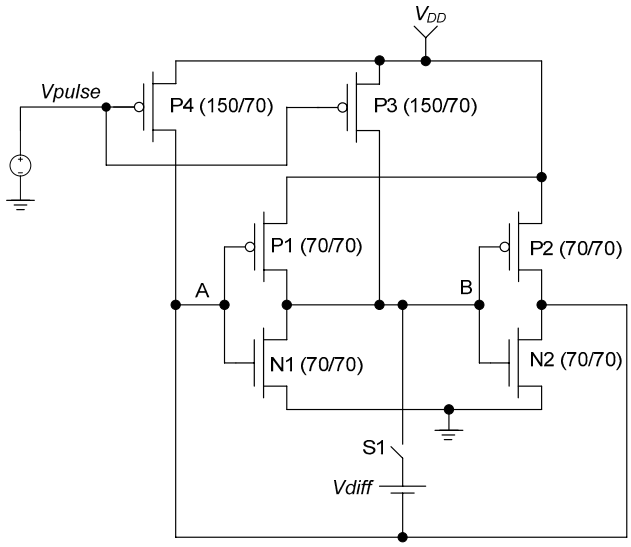

Figure 13 Symmetric boost latch - simulation circuit

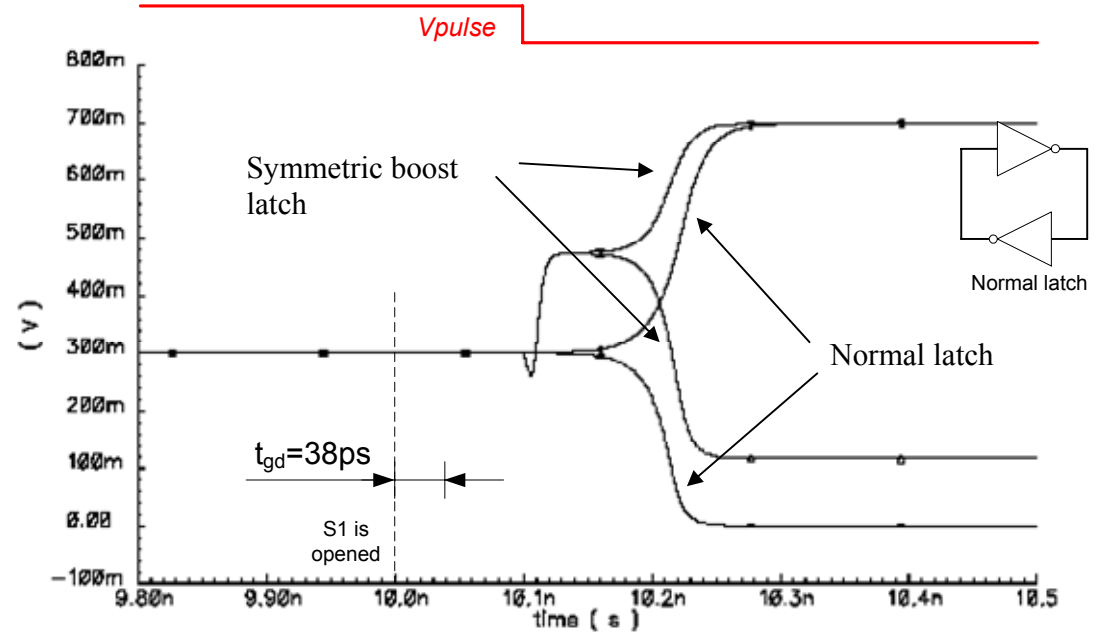

Figure 14 Transient analysis, V_{DD}=0.7V, T=27°C

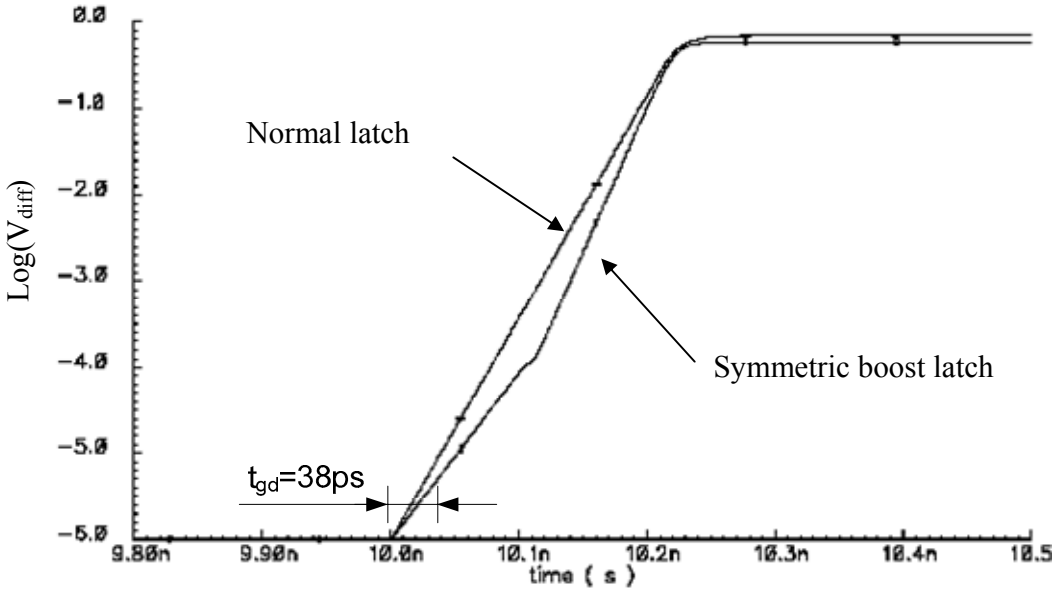

Figure 15 τ calculation, V_{DD}=0.7V, T=27°C. τ (symmetric boost)=13ps, τ (Normal latch)=16ps.

As one can see, at relatively high supply voltage the time constants of both circuits are almost identical (after applying the pulse), with slight advantage to the symmetric boost. When the supply voltage drops, the symmetric boost latch clearly outperforms the normal latch. The simulations in Figure 16—Figure 19 were performed at V_{DD}=0.4V ($2\times V_{th}$) and V_{DD}=0.35V.

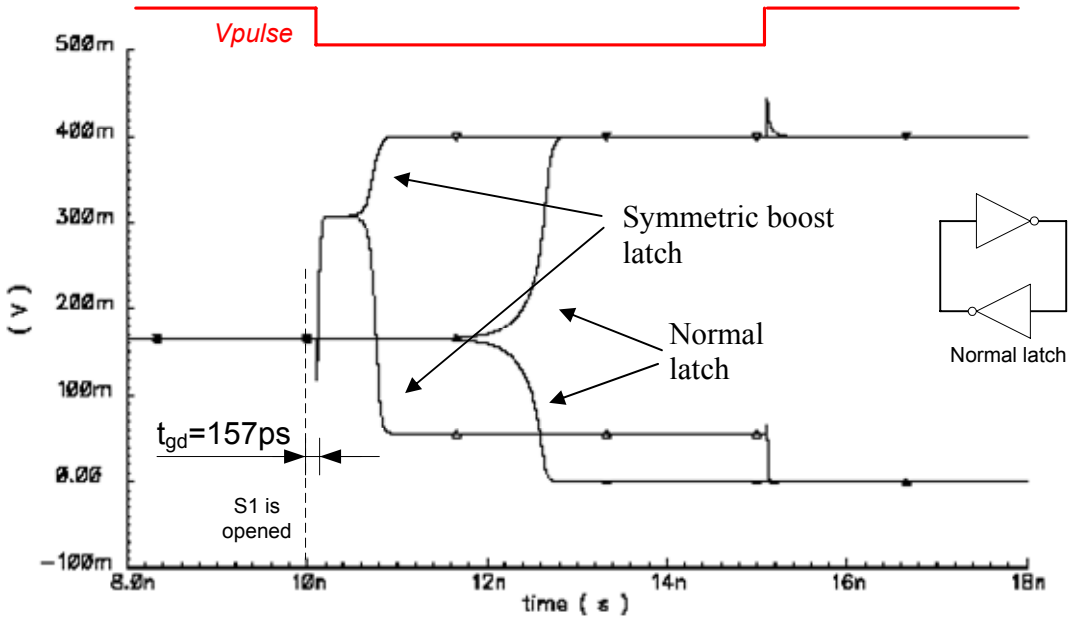

Figure 16 Transient analysis, V_{DD}=0.4V, T=27°C

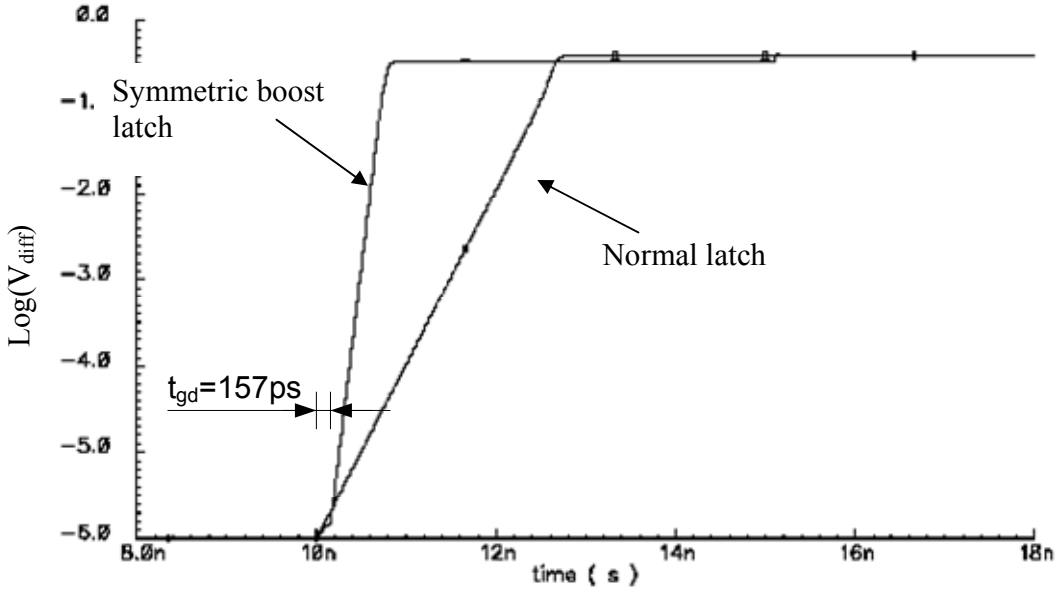

Figure 17 τ calculation, V_{DD}=0.4V, T=27°C. τ (symmetric boost)=50ps, τ (Normal latch)=214ps.

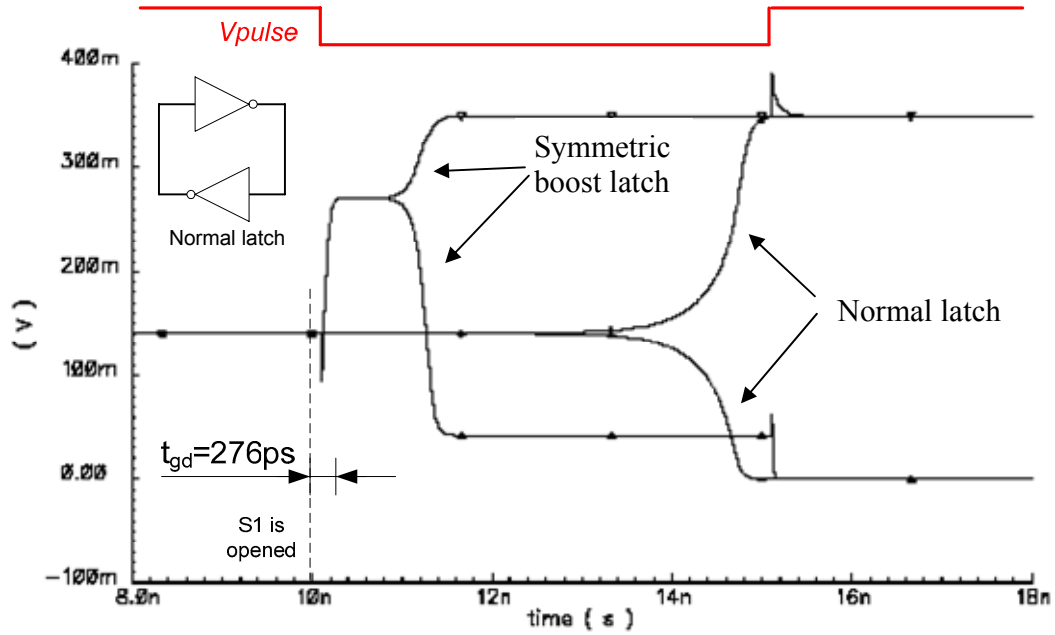

Figure 18 Transient analysis, V_{DD}=0.35V, T=27°C

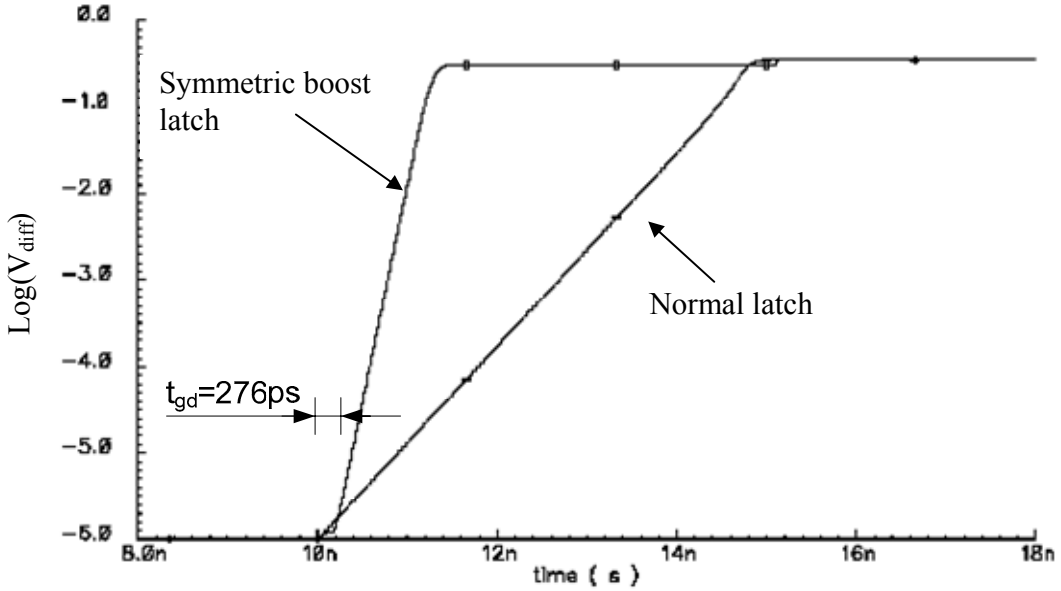

Figure 19 τ calculation, V_{DD}=0.35V, T=27°C. τ (symmetric boost)=87ps, τ (Normal latch)=388ps.

Next, low temperature of T=-20 ºC is considered in Figure 20—Figure 25. Other parameters are the same as above. Note the growing advantage of the symmetric boost latch over the normal one.

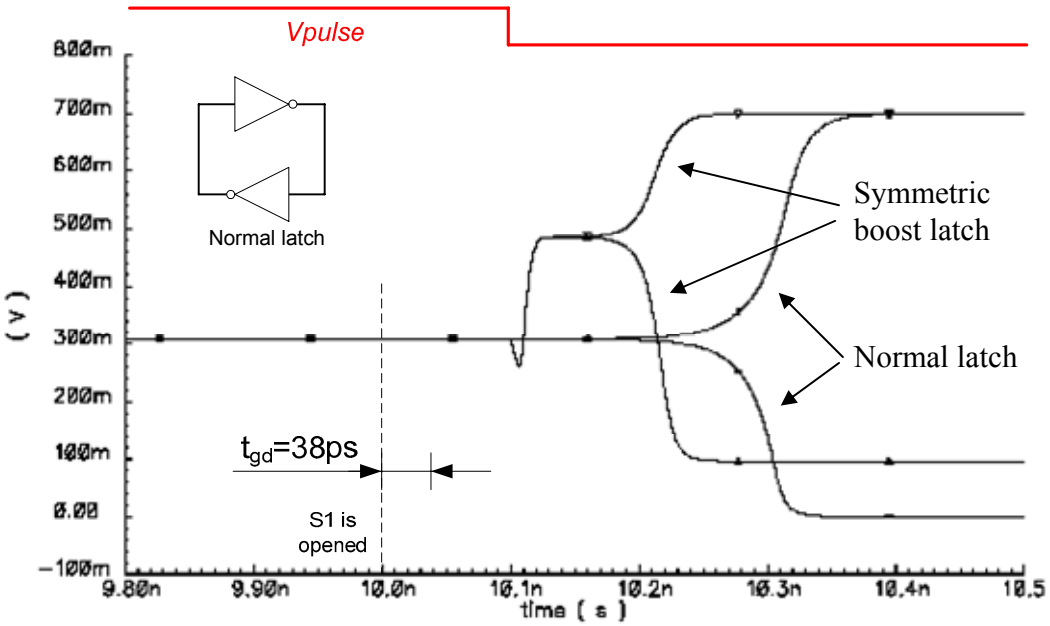

Figure 20 Transient analysis, V_{DD}=0.7V, T=–20°C

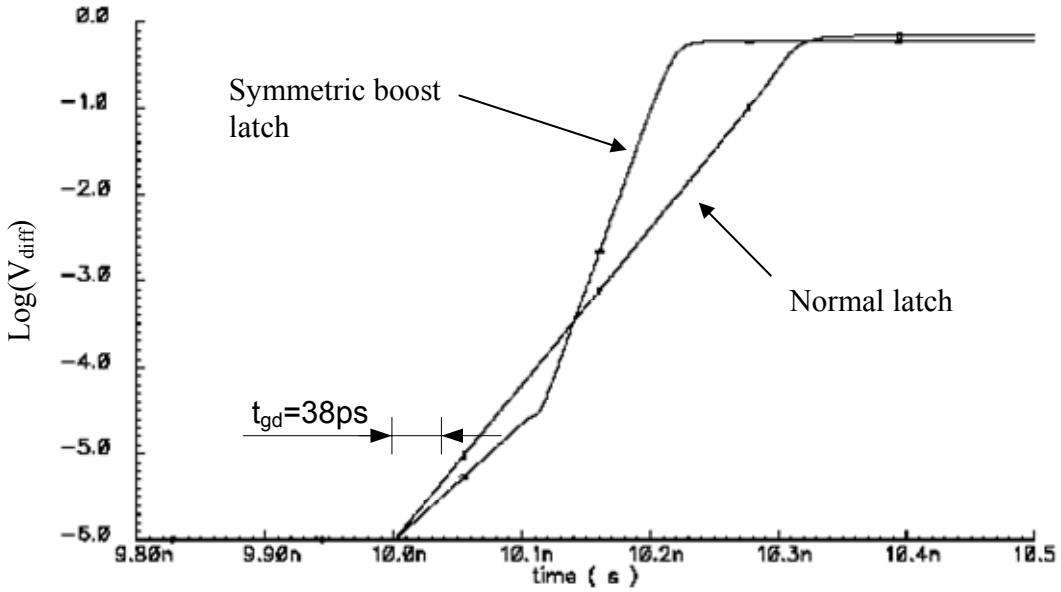

Figure 21 τ calculation, V_{DD}=0.7V, T=–20°C. τ (symmetric boost)=11ps, τ (Normal latch)=24ps.

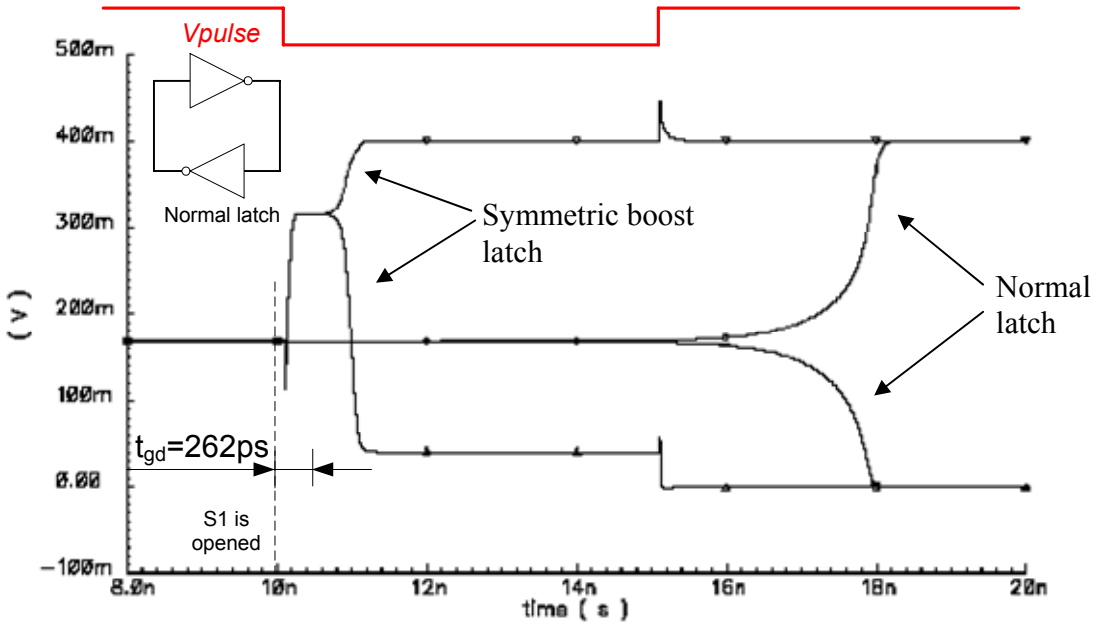

Figure 22 Transient analysis, V_{DD}=0.4V, T=–20°C

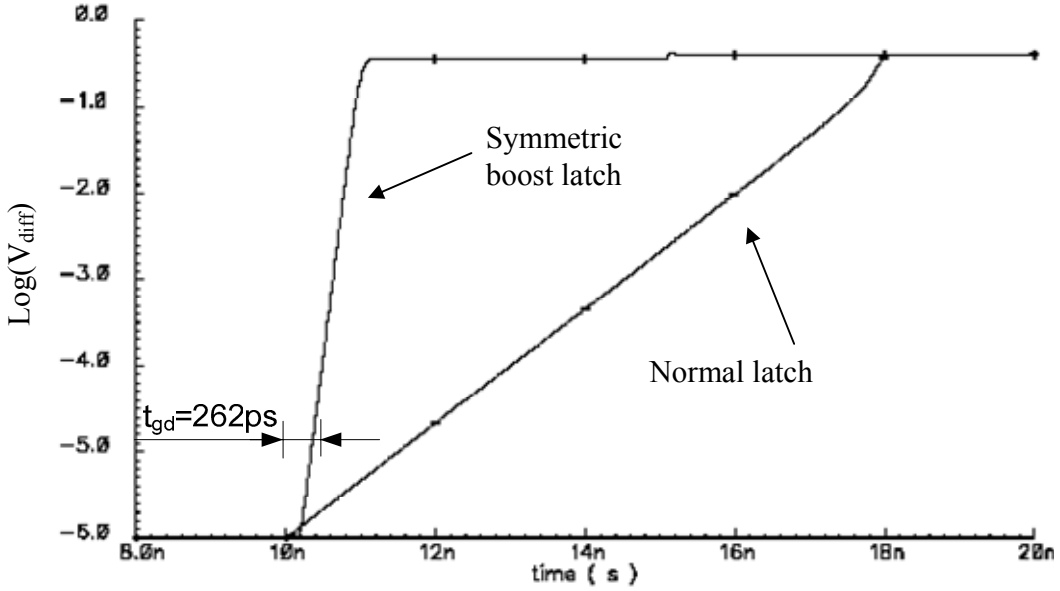

Figure 23 τ calculation, V_{DD}=0.4V, T=–20°C. τ (symmetric boost)=63ps, τ (Normal latch)=651ps.

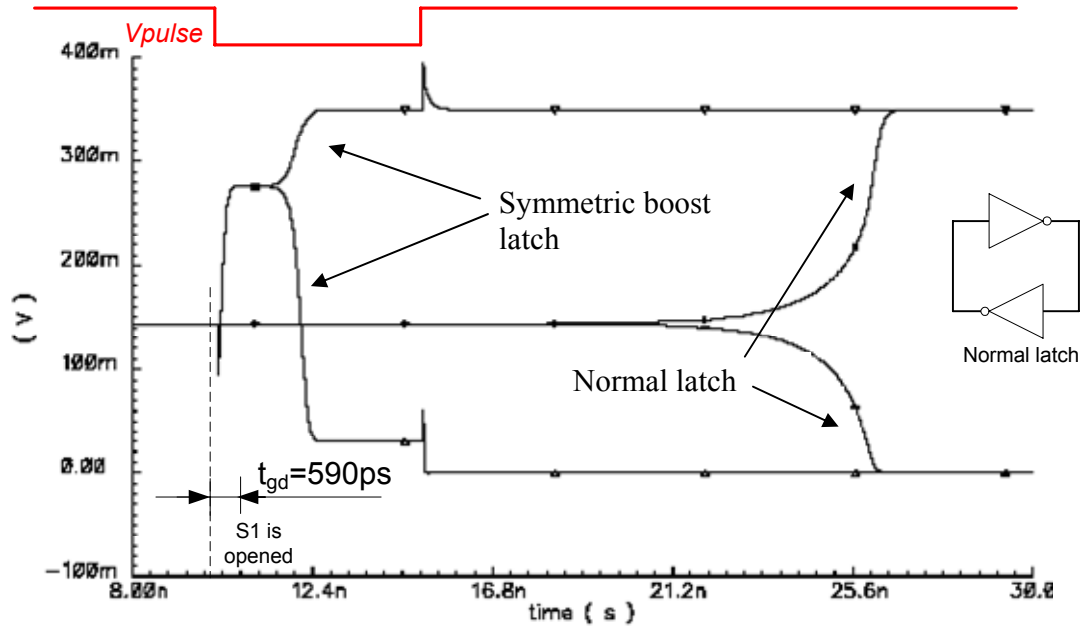

Figure 24 Transient analysis, V_{DD}=0.35V, T=–20°C

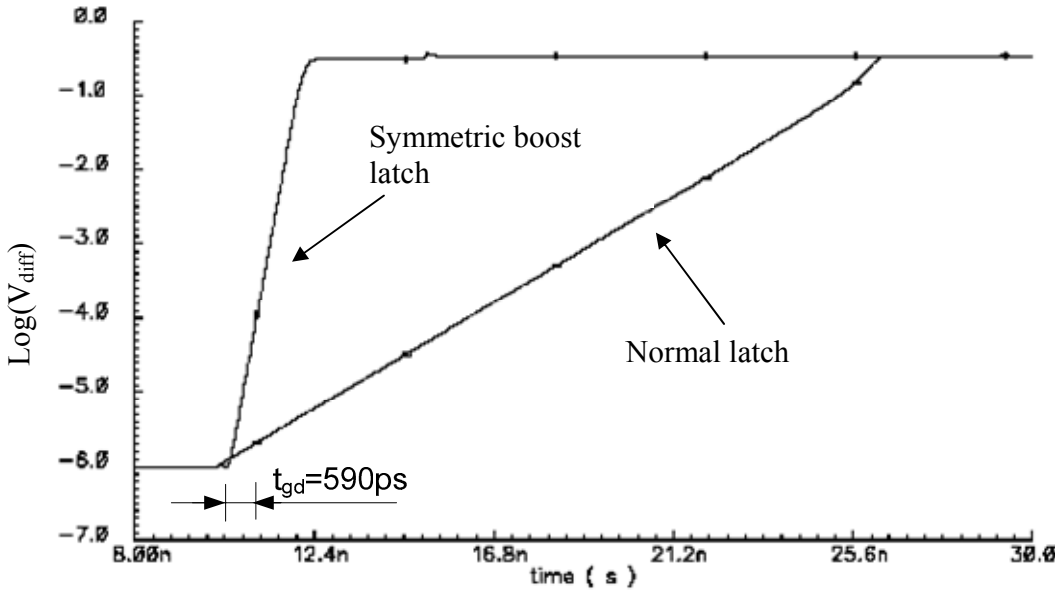

Figure 25 τ calculation, V_{DD}=0.35V, T=–20°C. τ(symmetric boost)=144ps, τ(Normal latch)=1332ps.

It is evident that the symmetric boost latch outperforms the normal latch under all these extreme conditions. The results are independent of the initial metastability starting voltage. To demonstrate this finding, simulations were performed at temperature T=-20 ºC, V_{DD}=0.4V and *Vdiff* varying over 11 decades from 1pV to 10mV, once per decade.

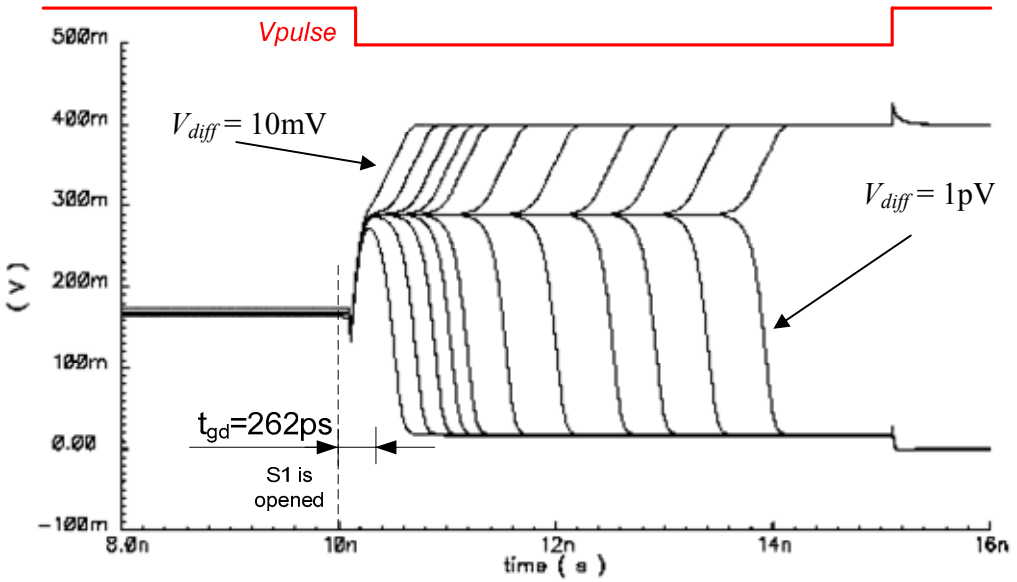

Figure 26 Transient analysis of the symmetric boost latch, V_{DD}=0.4V, T=–20°C V_{diff} varying over 11 orders of magnitude (1pV—10mV)

As can be seen, for virtually any value of *Vdiff* the latch manages to resolve quickly enough, even under conditions of low temperature and low supply voltage.

In order to examine the symmetric boost latch behavior at high supply voltage, the circuit was also simulated at V_{DD}=1.2V and T=27 ºC. The results are presented in Figure 27 and Figure 28.

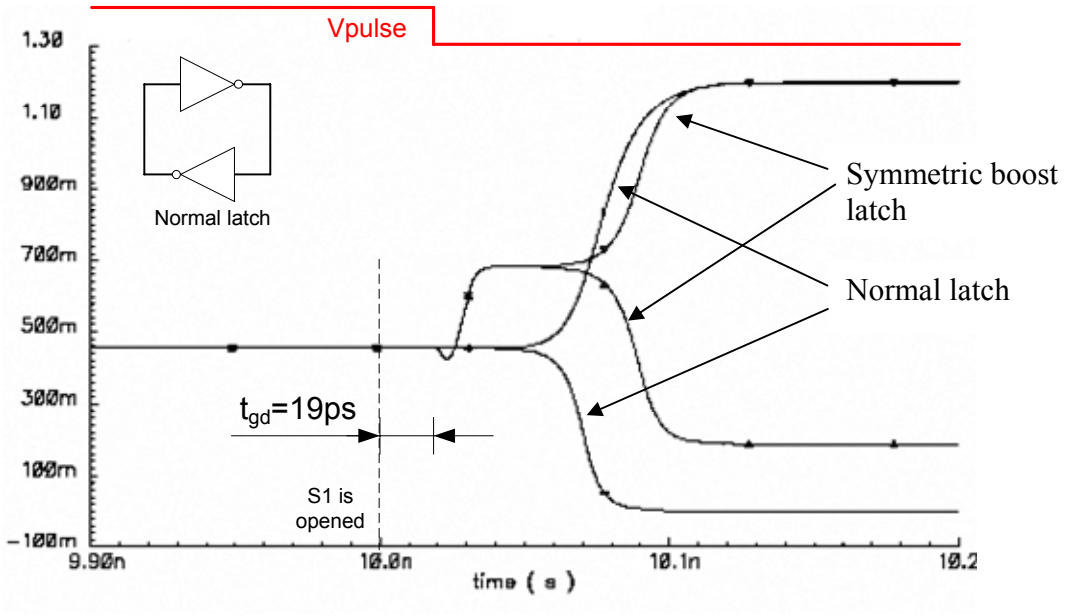

Figure 27 Transient analysis, V_{DD}=1.2V, T=27°C

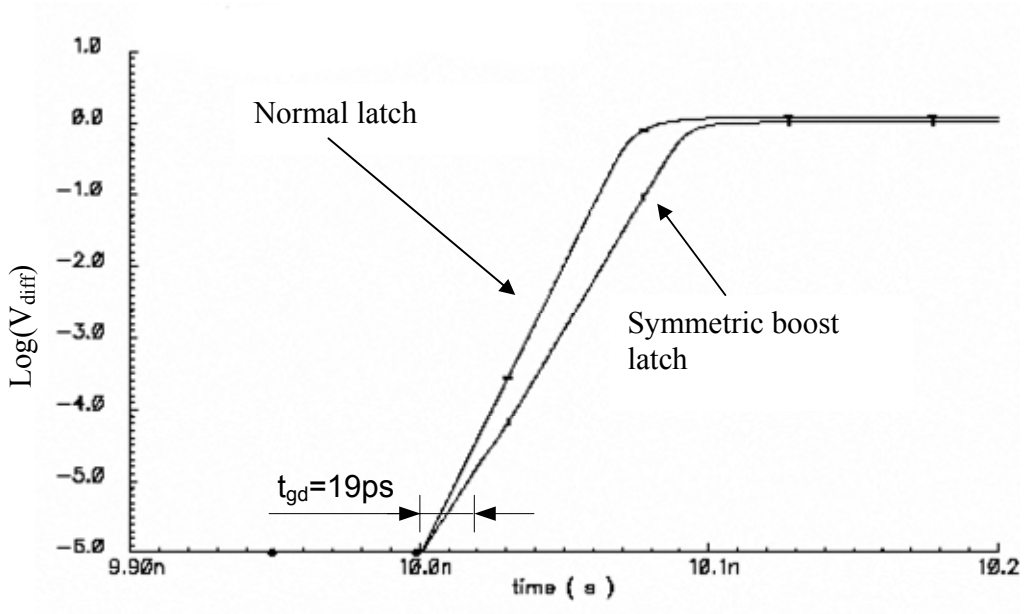

Figure 28 τ calculation, V_{DD}=1.2V, T=27°C. τ (symmetric boost)=6.4ps, τ (Normal latch)=5.1ps.

The corollary of the simulations is that the symmetric boost latch is most suitable for operating at low supply voltage and/or low temperature. At higher supply voltages the performance of the symmetric boost latch and the normal latch are almost identical.

5. Conclusions

We have shown that the symmetric boost latch can reliably synchronize over a very wide range of supply voltages and temperatures. The adverse effects of low supply voltage and low temperature on delay and synchronization were reviewed. As expected, the metastability resolution time constant τ of normal latches significantly increases at low supply voltage (~$2V_{th}$). At low temperature this problem is more severe, because V_{th} increases as the temperature drops. The symmetric boost latch exhibits much better performance than the normal latch. It was simulated and found capable of operating under conditions of very low temperature and low supply voltage. The charts in Figure 29 and Figure 30 demonstrate the superiority of the symmetric boost over the normal latch in terms of τ and MTBF at the low supply voltage of V_{DD}=0.4V, about $2V_{th}$, and over the wide temperature range of –50° to +150°C.

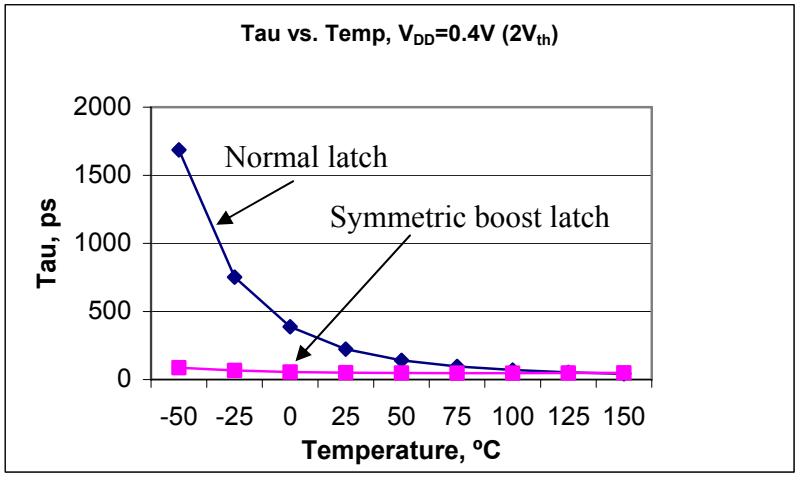

Figure 29 τ comparison

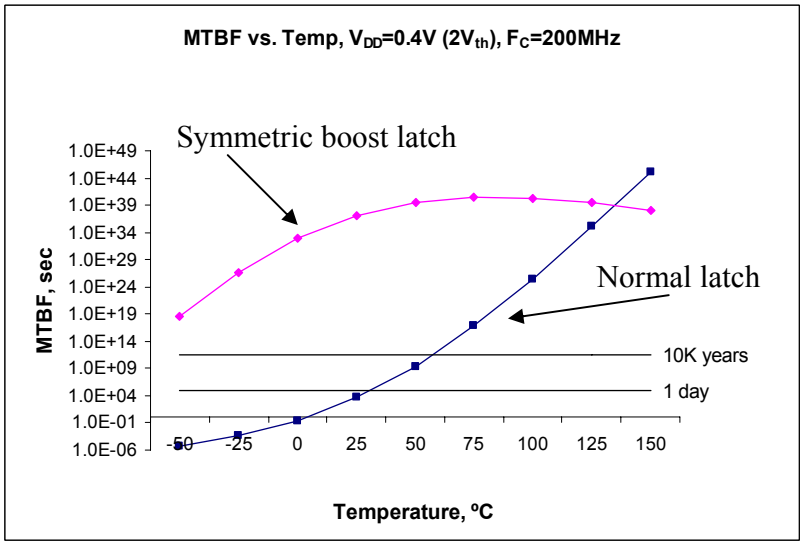

Figure 30 MTBF comparison

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