Structures of polymer field-effect transistor: Experimental and numerical analyses

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We compare two basic organic field-effect transistor structures both experimentally and theoretically. By using time-resolved analysis, we gain insight into the mechanisms affecting the performance of these structures. Using a two-dimensional numerical model, we focus on the top contact structure and analyze the difference between the two structures. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1431691]

Organic field-effect transistors (FETs) have been gaining attention over the past years. It seems that these transistors are outbreaking their performance and becoming very attractive for a range of applications. These are oscillators,[1] flexible devices,[2] smart cards/tags[3] small or large scale,[4] or even integrated optoelectronic devices.[5,6] Various device structures are often used to extract material properties with the common assumption that the unique structure of organic transistors ''behaves'' just like standard Si metal–oxide–semiconductor-field-effect transistors. Most indepth studies are usually focused on material issues[7] while in this letter, we focus on device-structure related effects. In Ref. 8 we numerically studied the physical mechanisms related to organic FETs while in this letter, we demonstrate the effect on the current–voltage ($I-V$) curves. Specifically, this letter describes experimental and numerical comparison of two relevant FET structures: (Fig. 1) the top contact (TOC) and bottom contact (BOC) structures.

Figure 1 describes the FET structures that are being considered. The substrate consists of heavily doped p-type Si (gate) and thermally grown SiO_2 (gate insulator). The polymer used was MEH-PPV (ADS-100RE as supplied by ADSDYES).[9] Solutions of 7 mg/ml in toluene were prepared and spincoated in an inert glove box (below 1 ppm of oxygen and water) followed by thermal annealing under a dry vacuum (within the glove box) at 90 °C for 30 min. The active layer (MEH-PPV) thickness was below 100 nm. In the BOC structure, an interdigitated gold source and drain contacts are defined using standard photolithography and the device is finished by spin coating the active polymer. In the TOC structure, we first spin coat the active layer and later thermally evaporate through a shadow mask two stripes of gold that define the source and drain contacts (slow evaporation at 3×10^{-7} mbar). All $I-V$ curves, as well as time dependent curves, were measured using a HP semiconductor parameter analyzer. In the numerical simulation, the film thickness is 50 nm, and for the convenience of the simulation the insulator thickness was made the same. The mobility was assumed to be 5×10^{-3} $cm^2\ V^{-1}\ s^{-1}$. The drain–source distance (channel length) is 5 μm which is much larger then the film thickness. The same holds for the size of each source/drain contact being 1 μm. The simulation extends a few microns beyond the source drain contacts to reduce edge effects. The simulated channel length was chosen due to numerical convergence requirements and has no significant bearing on the results shown (see also Ref. 8) and the features compared to the experimental 40 μm channel length. More details of the simulation program can be found in Ref. 8.

Figure 2 describes the measured drain current as a function of drain–source voltage for a range of gate bias voltages. Both the BOC and the TOC structures show well-defined saturation behavior and using the standard FET equations the extracted mobility values (from the saturation regime) are 5×10^{-5} and 8×10^{-5} $cm^2\ V^{-1}\ s^{-1}$ for the TOC and BOC structures, respectively. Despite the almost identical mobility value, we note that in the TOC case the ''linear'' regime exhibits super linear rise with a (positive) offset at low drain–source voltages. A super-linear behavior is often explained as the effect of a contact barrier at the polymer metal interface. For the current experiment, this is not likely to be the case as gold generally forms a good hole-injection contact to MEH-PPV devices.[10] Moreover, the BOC device, which employs the same contact metal, shows no trace of this super-linear dependence. These results suggest that the

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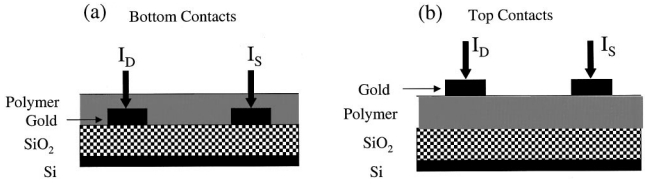

FIG. 1. Schematic description of TOC and BOC FET structures.

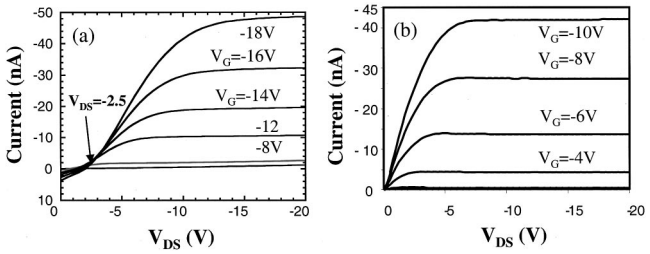

FIG. 2. Measured drain current for TOC (a) and BOC (b) structures. The channel lengths were 40 μm and 10 μm respectively.

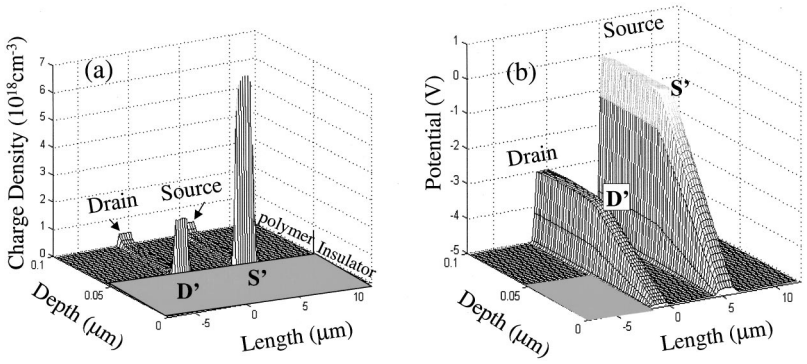

FIG. 3. Calculated 2D distribution of the hole density (a) and the electrostatic potential (b) 150n after the gate bias was set to -5 V ($V_S=0$, $V_D=-3$ V).

TOC structure requires deeper examination and hence we apply our two-dimensional (2D) model to it next.

To set up the scene for the internal operation of the TOC FET, we first simulate the turn on of the FET. Namely, the device was kept at $V_G=V_S=0$ and $V_D=-3\ V$ and at $t=0$, the gate voltage was changed to $V_G=-5\ V$. Figure 3 shows the calculated 2D distribution of the hole density [Fig. 3(a)] and the electrostatic potential [Fig. 3(b)] 150n after the gate bias was set to $-5\ V$ ($V_S=0$ and $V_D=-3\ V$). We note that at this short delay time, both source and drain contacts inject charges into the structure and charge the region under the contacts [Fig. 3(a)]. Figure 3(b) shows that a successful charging results in the potential being flat across the polymer layer and the applied source and drain potentials are imaged onto the insulator boundary. The charge density under each contact is proportional to the applied bias between the given contact and the gate electrode ($Q=C^*\Delta\ V$). In the ideal case, we could say that virtual contacts have been formed at points S' and D' (see Fig. 3) next to the insulator boundary. In this ideal case, one would expect the TOC device to ''behave'' as if the gold electrodes were deposited on the SiO_2 directly (i.e., BOC device). However, this is not so since for the current to flow out of the drain contact, the potential at D′ must exceed, if only by little, that of D. Moreover, it is not always the case that $V_{S'}=V_S$ or $V_{D'}=V_D$. As stated above,[8] for these equalities to hold a certain charge-density must be formed at the insulator boundary (i.e., successful charging). Regarding the drain contact, we note that the required density is higher for lower V_{DS} bias (as V_{DG} becomes larger).

Using a complete set of results, we found that the mechanism that may prevent the charge under the contacts to reach its full value is a parasitic charging current. In this case, the charging is of the rest of the device structure namely, the device periphery or the insulator interface across the substrate. When the charging of the outer regions is pronounced, it behaves like a small leakage current that prevents full charging of the area under the contacts (as if a resistor was placed in parallel with the gate capacitance). In this case, the charge density at the insulator does not reach its optimum value and hence the potential at points S' and D' can not exceed a certain value ($V_{D'\,\max}$, $V_{S'\,\max}$). The situation is mostly critical under the drain as for the current to flow from the source to the drain, the potential at D' must exceed, if only by little, that of D and this can only occur if the source would be able to support (through the channel) a high enough density under the drain (at D').

An example of the case where the source can not support a high enough density, was simulated by slightly enhancing the contact barrier so as to amplify the effect of the charging current (increasing the channel length will create a similar effect here). To make things ''worse,'' we lowered the source drain bias so as to increase the required density at D' (by increasing V_{DG}). Figure 4(a) shows the potential distribution once the region under the contacts and in the channel has reached its steady state (the rest of the substrate is still charging). We notice that there is a slight voltage drop under the source due to the slightly enhanced contact barrier ($V_{SS'}=0.5-0.6\ V$) but a more pronounced one at the drain ($V_{D'D}\cong-1.5\ V<0$). As the current supplied by the source, through the channel, to the drain region was reduced it could no longer successfully compete with the charging current. This results in the density (and potential) at D' being limited and $V_{D'D}$ being negative. It is clear that in this case I_D is positive [see offset in Fig. 2(a)] and no current is flowing from the source and out of the drain. The potential-pinning effect is also demonstrated using the schematic potential diagram in Fig. 4(b). In this schematic illustration V_D is varied from zero to V_G. We note that only when V_D will go below a certain value [$V_{D'\,\max}=-2.5$ V in Fig. 4(a)] will a current flow from the source and out of the drain.

In other words, the charging of the insulator interface formed an effective potential barrier under the drain elec-

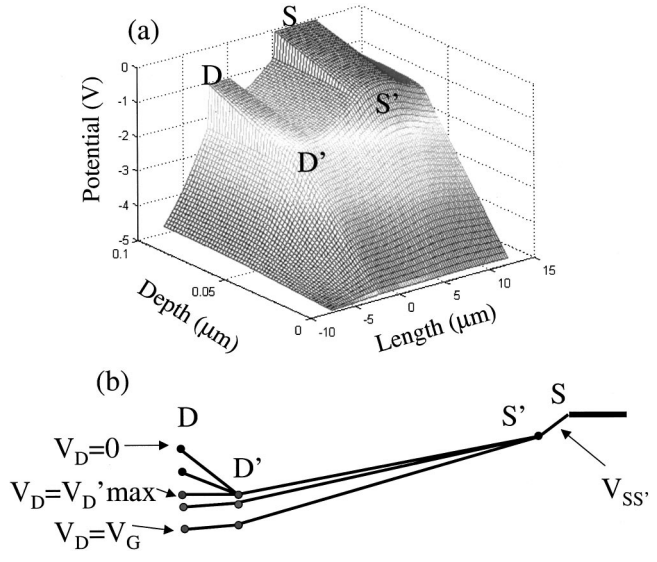

FIG. 4. (a) Calculated 2D potential distribution for the TOC structure. The transistor active region has reached its steady state. (b) Schematic description of the potential distribution between the contacts for varying drain voltage.

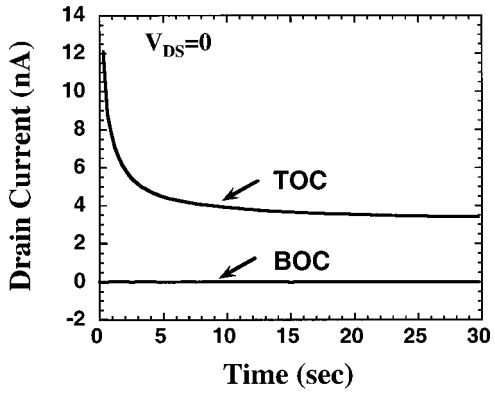

FIG. 5. Measured drain current as a function of time after applying a gate bias. TOC curve was measured in the TOC structure and the BOC curve for the BOC one.

trode. It may very well be that this is indeed the mechanism that produced the super-linear curves in Fig. 2(a). To test this hypothesis, we had to verify whether our TOC structure exhibits pronounced charging effects. To do so, we time resolved the current flowing through both the source and the drain electrodes. Figure 5 shows the measured drain currents for the BOC and TOC structures as a function of time in response to a step in the gate voltage. We note that although $V_{DS}=0$, the drain current for the TOC device is positive (into the device) and remains so for a long time. The initial ''fast'' drop has an RC time corresponding to the injection resistance (metal contact+polymer layer) and the capacitance under the contacts. The long tail is due to the charging (capacitance) of the device periphery. Namely, there is a pronounced charging of the device with about 4–5 nA at the end of the measurement (see also Fig. 2). For the BOC case however, the measured current is limited by our instrument response and it fluctuates around zero (± 10 pA). This clearly demonstrates that a pronounced difference between the TOC and BOC devices presented here is indeed that of charging effects.

In conclusion, we have demonstrated the difference between two widely used organic FET structures using both experiment and numerical modeling. It was demonstrated that for TOC devices the charging of the insulator interface might form an effective potential barrier under the drain electrode. If ignored, this may lead to the erroneous evaluation of the material parameters. In cases where the simplest method, of buying a Si/SiO_2 substrate, spinning a polymer on, and depositing top contacts, is used to screen or optimize materials, good materials may be abandoned. We found the time-resolved measurements to be essential for the evaluation of organic FETs (especially when a new material or device structure is involved). Better insight into the operation of organic structures will lead to enhanced structures on one hand and modified semi-analytical expressions on the other.

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