Turn-on and Charge Build-up Dynamics in Polymer Field Effect Transistors

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ABSTRACT

Turn-on dynamics of polymer field effect transistors were examined experimentally over a wide timescale. We found that the source current dependence on time following switch on of the gate bias exhibits a power law at the short time range, and an exponential decay at the intermediate to long time range. We demonstrate that the transistor dynamic behavior is governed by the channel charge build-up, and can be described accurately by a simple capacitor-resistor distributed line model.

INTRODUCTION

Time response of field effect transistors (FETs) after an abrupt change of gate bias (switch-on/off) is often assumed to be governed by the transit time of charge across the channel, or by residual capacitances charging [1]. Recently, it has been demonstrated that channel charge rearrangement determines the switch-on time in low-mobility FETs, made of conductor, insulator and a π-conjugated active layer (CIπ-FETs) [2]. It has been found that the source current follows an exponential dependence on time, at the time range which is close to the switch on time. In this work we examined the dynamics of the channel charge build-up after the switch-on in a CIπ-FET, over a wide time range.

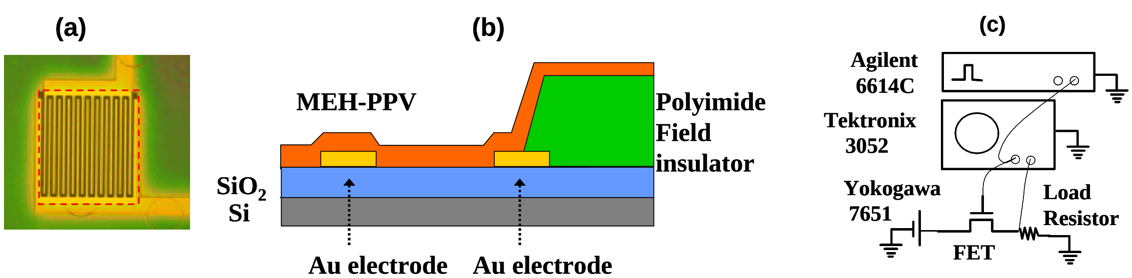

Figure 1: Top view (a) of MEH-PPV PFET with periphery current reduction by polyImide field insulator. The active area, marked by a dashed line in (a), is surrounded by field insulator, as plotted in the schematic cross section near the active area edge (b). The time response measurement setup is given in (c).

EXPERIMENTAL DETAILS

We examined poly-[2-methoxy-5-(2 '-ethyl-hexiloxy)-p-phenylenevinylene] (MEH-PPV, American Dye Source ADS 100RE) bottom contact PFET (Figure 1). The dimensions of the transistors are $W = 6000\ [\mu m]$, $t_{ox} = 67$ [nm], $L = 5.5$, 9.5, and 17.5 $[\mu m]$. We used high molecular weight polymer (MW=1M [gr/Mole]) to obtain high mobility[3]. In order to decrease the charging current of the periphery[4] we used a PolyImide field insulator (Figure 1) beyond the external electrode of the active area (The PolyImide layer was etched prior to the electrode lithography in order to prevent damage to the gate oxide). More details of the MEH-PPV PFET properties and design are given elsewhere [5].

The DC characteristics of the 17.5 $[\mu m]$ channel CIπ-FET (Figure 2) were carried out in a glove box using semiconductor parameter analyzer, Agilent HP4155C. The high concentration mobility value ($\mu = 2 \cdot 10^{-4}$ $[\mathrm{cm}^2 / V\,\mathrm{sec}]$) was extracted from the saturation current. The switch-on voltage [6] of the transistors was stable during the time resolved measurements ($\mathrm{V}_{\text{Switch-on}} = 3.2 \pm 0.1 \left[\mathrm{V}\right]$), and the contact resistance in this device was negligible for the entire gate bias range. Time resolved measurements at the time range between nano-seconds and seconds were carried out using the following set up (Figure 1.c): The source drain bias was held by a power supply unit (Yokogawa 7651), while the gate bias was switched by a pulse generator (Agilent 6614C). The current in the transistor was measured by a scope (Tektronix 3012) probing the potential drop on a load resistor. All of the measurements were carried out in the glove box without exposing the CIπ-FETs to air.

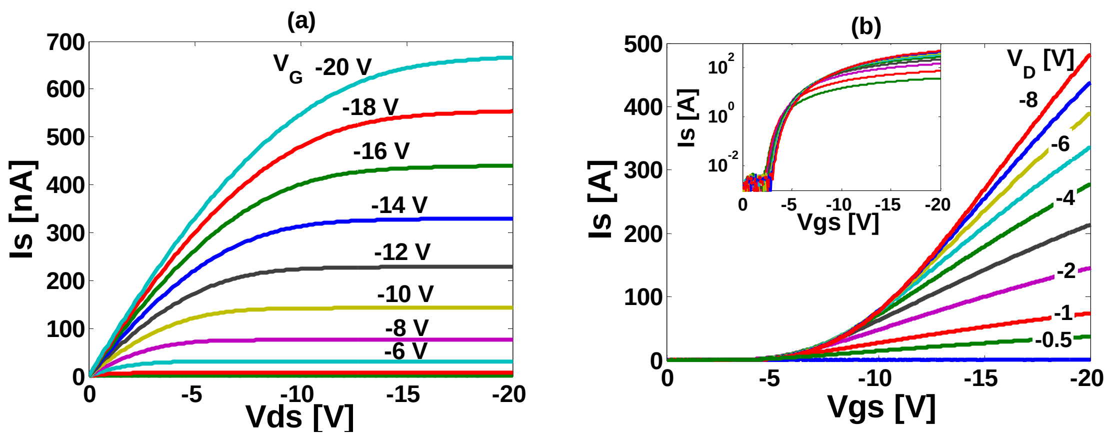

Figure 2: Conductance (a) and transconductance (b) characteristics of 17.5 $[\mu m]$ channel MEH-PPV CIπ-FET. (The saturation mobility $\mu_{sat} = 2 \cdot 10^{-4}$ $[\mathrm{cm}^2 / V\,\mathrm{sec}]$)

RESULTS AND DISSCUSION

Time resolved electrodes currents, after gate bias was switched from 0 V to -8 V, where the drain source bias was kept constant (V_{DS}=-8 V) are given in Figure 3. The load resistor was changed from 100 Ω to 10 kΩ in order to vary RC time constant while maintaining a reasonable signal to noise ratio. By this method we were able to expand the examined time range (down to the RF attenuations of the measurement lines). We find that over a large timescale the source current decreases monotonically, and the drain current is very low and opposite in sign to the DC drain current. After a long decay of the source current it stabilizes at the DC value, at t_{on} (Figure 2). Adjacent to t_{on} the drain current rises abruptly to its DC value as the transistor switches from "close" to "open". The source current decrease follows power law dependence over a large time range (approximately three decades). The switching time exhibit a scaling law with the squared channel length (insert in Figure 3). This scaling law can be applied to any intermediate situation of current, namely, all of the source current curves can be described by a single master curve that depends upon the normalized time ($t_{normalized} = t / L^2$). As the current before the switch-on time is necessarily the channel charging current, this scaling law can be simply explained using the following argument: The total charge of the channel is proportional to channel length, and the momentary electric field, and therefore the current are proportional to the inverse channel length (assuming constant mobility). Therefore the switch-on time is proportional to the channel length squared ($t_{on} \sim Q/J \sim Q/E \sim L^2$).

The observation of a power-law decay of the current is significantly different than the exponential decay observed at relatively long time scale and small signal that was reported in Ref. [2]. Such an exponential decay was observed in our measurement only at times adjacent to the switch-on time. These observations (the power law current decay at short time scale and the exponential decay near t_{on}) were predicted by a two dimensional Poisson - continuity equations numerical results (described elsewhere [4, 7]). Such calculations however, are complex and time consuming. Here we present a simple approach that describes the CIπ-FET transient behavior at moderate and high biases, where the mobility can be regarded as almost constant and independent of the charge concentration or applied electric field.

Our approach relies on a distributed transmission line presentation of the channel. In this approach the channel is presented by a series of resistors and capacitors (R_i and C_i, respectively, see insert in Figure 4.a). This presentation is convenient to apply in VLSI numerical simulators, as the transistor is replaced by a simple equivalent circuit composed of linear elements. We note that a continuum approach, similar to ours was presented in Ref. [2]. However it was fully solved only for limited conditions, namely where variable separation can be applied. This assumption is applicable only for small signal, and for this reason it is applicable only to describe the exponential decay at the end of the charging (close to the switch-on time). As demonstrated by the time resolved measurements, and the full solution demonstrates (see Figure 3 in Ref. [4]) and

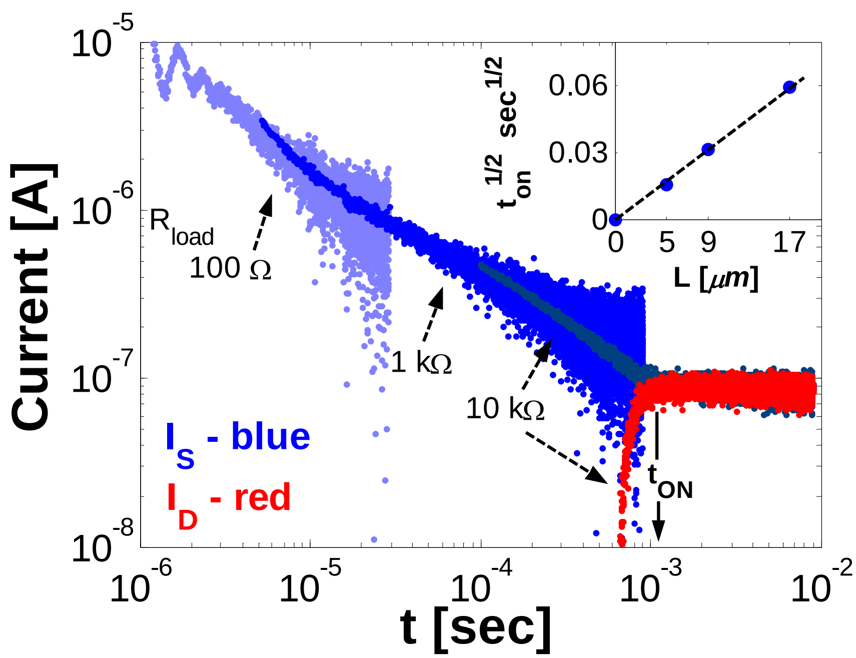

Figure 3: Measured source (blue) and drain (red) currents of PFET after switching the gate voltage from 0 V to -8 V where the drain voltage was kept at constant bias (V_{DS}=-8 V). The switching time (t_{on}) is the time that drain current reaches its DC value, the channel charging is completed and the source and the drain currents are equal. The switch on time is scaled with the squared channel length (see insert).

as we found in the distributed line calculation (Figure 4), this assumption is not valid for short times, where the current decays according a power-law. For this reason we developed a general approach for the solution of the current and potential dependence on time.

The solution is based on a distributed line of capacitors and resistors of the CIπ-FET channel, where the mobility is assumed to be independent of charge concentration ($\mu(p) = Const = \mu_{sat}$). R_i are the serial resistance associated with the current that flows through, and fill up, the channel. The resistance, R_i, is derived from the conductivity as:

$$R_i = \frac{\Delta L}{A}\frac{1}{q\mu p} = \frac{\Delta L}{d_\pi * W}\frac{1}{q\mu p} \tag{1}$$

where d_π is the accumulation layer width[7], ΔL is the distance separating two elements. The charge density p is determined by the voltage that drops across the capacitors next to R_i:

$$R_i = \frac{\Delta L}{d_\pi * W}\frac{1}{q\mu\frac{C_{ins}\frac{V_i + V_{i+1}}{2q}\Delta L * W}{d_\pi * \Delta L * W}} = \frac{\Delta L}{W}\frac{1}{\mu C_{ins}\frac{V_i + V_{i+1}}{2}} \tag{2}$$

To solve the equivalent distributed line of the channel we require defining the boundary conditions:

$$\begin{cases} V_1 = V_S ; V_{n+1} = V_D ; \\ for\ i \neq 1, n+1\ V_i\big|_{t=0} = 0 \end{cases} \tag{3}$$

and for the dynamics of the system we rely of the capacitor characteristics $\left(I_i = c\frac{dV_i}{dt}\right)$ and on Kirchof law $I_i = I_{R_{i-1}} - I_{R_i}$:

$$\frac{dV_i}{dt} = \frac{1}{C_{ins} \cdot W \cdot \Delta L}\left(\frac{V_{i-1} - V_i}{R_{i-1}} - \frac{V_i - V_{i+1}}{R_i}\right) \tag{4}$$

As we assumed that μ is field and density independent we arrive at an expression similar to the continuous form[2]:

$$\frac{dV_i}{dt} = \frac{\mu}{2\Delta L^2}\left(V_{i-1}^2 - 2V_i^2 + V_{i+1}^2\right) \tag{5}$$

and finally the transient currents are:

$$I_S(t) = \frac{V_S - V_2(t)}{R_1} \qquad I_D(t) = \frac{V_D - V_n(t)}{R_n} \tag{6}$$

The above equations suggest that the transistor switch on characteristics are rather universal and only depend on the channel length, the material mobility, and the insulator capacitance (where the last only determines the absolute value of the current, but not the time dependence). In Figure 4 the charge concentration distribution in the channel (that is linearly dependent on the potential distribution) is plotted for different time after voltage switching. It is clear that at the short time range a solution that relies on variable separation (namely, $V(x,t) = X(x)T(t) + f(x)$) cannot be applied (e.g. the distribution decay point varies on time).

We identify two situations: Gate switching bias that is (a) in the saturation range ($|V_{GS} - V_T| \leq |V_{DS}|$), and (b) in the linear range ($|V_{GS} - V_T| > |V_{DS}|$). In the first situation (Figure

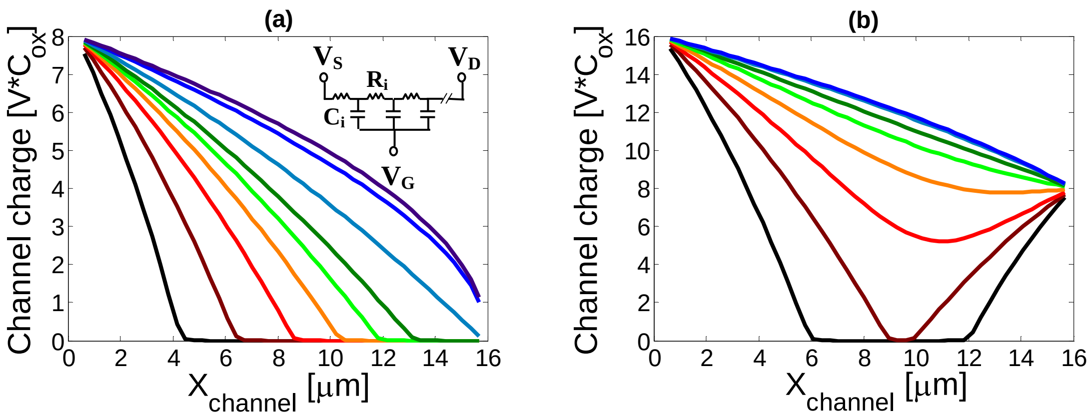

Figure 4: Transmission line method (TLM) Calculated surface charge in the FET channel at different elapsed times after operating gate bias for: (a) low drain voltage ($|V_{GS}-V_T| \le |V_{DS}|$, $V_{GS}=V_{DS}=-8$ [V], $V_T=0$), and (b) high gate voltage ($|V_{GS}-V_T| > |V_{DS}|$, $V_{GS}=-16$ [V], $V_{DS}=-8$ [V], $V_T=0$). The colors at both graphs present the same elapsed time after gate bias switching.

4.a.) the charging is only from the source and the drain charging is negligible. This result in one slope (nominator) in the log-log current-time curve. On the other hand, when the switching is to the triode (linear) range of the transistor (Figure 4.b.) the charging is both from the source and the drain. When the charge "frontier" that advance from the source meet the charge "frontier" from the drain, the source current decays faster toward the DC source current, and the slope of the log-log current-time curve changes and the curve becomes steeper. This can be seen in both measurement and calculation (Figure 5). All of the calculated curves are with the same parameters (and without additional free parameters): $\mu = 1.4 \cdot 10^{-4}$ [$cm^2/V\sec$], $V_T = -3.6$ [V] and $I_{noise} = 9 \cdot 10^{-8}$ [A]. We note that: 1) the "noise current" is originated from a slight bias difference at the load resistor due grounding potential difference. 2) The absolute threshold voltage is slightly higher than the absolute switch-on bias observed in the DC measurements. This can be explained by a sub-threshold current due to deep state, or charge concentration dependence of the mobility. 3) The fitted transient mobility is slightly lower than the saturation mobility ($\mu_{sat} = 2 \cdot 10^{-4}$ [$cm^2/V\sec$]), by a reason we are unable to explain.

Finally, note that the distributed line method and the Poisson-continuity solutions that describe the channel charging well, relies on a constant mobility approximation. It has been demonstrated before[3, 8-10] that the mobility in amorphous organic semiconductors varies strongly with charge density. Therefore one may expect that the transient curves will deviate from the universal, constant mobility shape. Nevertheless, except for the low gate bias curves that deviated significantly from the constant mobility approximation (lower curves in figure 5), the charging curves were successfully described over a wide range of biases and time by this model. We assume that the constant mobility is kept by the high voltage drop across the charge carrier front and by the relatively high charge concentration. These factors drive the mobility toward the maximum mobility value, that is expected by the variable range hopping (or polaronic) model[7, 10].

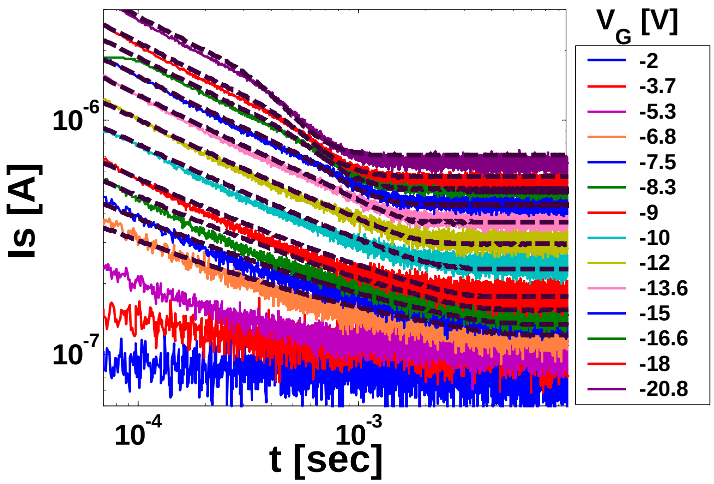

Figure 5: Experimental and transmission line simulation results (colored and dashed lines, respectively) of PFET charging current for different gate voltages (V_D=-8 [V]). All of the simulation are with the same parameters: $V_T = -3.6$ [V], $\mu = 1.4 \cdot 10^{-4}$ [cm^2 /V sec], and $I_{noise} = 9 \cdot 10^{-8}$ [A].

CONCLUSIONS

Polymer CIπ-FET current was measured over a large timescale following gate voltage switching. We found a power law decay of the source current on time over a wide range of time (more than three decades), followed by a short exponential decay, and an abrupt change from "off" to "on" state of the transistor, observed in the drain current. We have shown that distributed line model of capacitors and resistors can reproduce the experimental results at the high charge density regime and thus demonstrate that the dynamics are determined by the channel charge rearrangement.

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