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Patterned electrode vertical field effect transistor: Theory and experiment

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We present a theoretical and experimental investigation of the recently reported new architecture of a patterned electrode vertical field effect transistor (PE-VFET). The investigation focuses on the role of the embedded source electrode architecture in the device behavior. Current-voltage characteristics was unraveled through the use of a self-consistent numerical simulation resulting in guidelines for the PE-VFET architecture regarding the On/Off current ratio, output current density, and apparent threshold voltage. Current modulation characteristics are obtained through the formation of virtual contacts at the PE nano-features (i.e., perforations) under gate bias, which lead to the formation of vertical channels under drain bias. As the vertical channel is formed the device characteristics change from contact-limited to space-charge-limited. The analytical model strength is shown with the parameter extraction procedure applied to a measured PE-VFET device fabricated using block copolymer lithography and with the appropriate simulation results. © *2011 American Institute of Physics*. [doi:10.1063/1.3622291]

I. INTRODUCTION

Organic field effect transistors (OFETs) attract considerable interest, being flexible, low cost, and amenable to large area fabrication techniques. They are expected to integrate into the growing variety of organic electrical products such as flexible displays, sensors, and disposable devices with moderate computing demands (e.g., radio frequency identification tags). However, the inherent low mobility of the non-crystalline active material, 3 to 6 orders of magnitudes lower than that of crystalline materials, results in low performance in terms of current output, On/Off ratio and modulation frequency, which hinder the practical realization of these devices.

Vertical field effect transistor (VFET) architecture with the drain and source electrodes vertically stacked enables the reduction of channel length without substantial increase in cost or complexity of fabrication, and may compensate for the low mobility. These thin film transistors (TFTs) can be categorized into two groups. The first group can be referred to as semi-vertical devices, characterized with vertical fabrication but lateral structural configuration, i.e., the channel length is determined by the layers' thickness but the gate is still spatially located between the source and the drain electrodes.[1–6] The drain and source electrodes are either in the same layer[5,6] where the space is defined by surface topography, or in separate layers in which case the thickness of either the dielectric layer[2–4] or the active layer[1] defines the channel length. The second group is of "pure" VFETs where the gate, source, and drain electrodes are stacked vertically. The current-voltage characteristics of these devices cannot be described simply by the lateral devices physical picture, i.e., the gradual channel approximation,[7] where channel length, width, and dielectric capacitance constitute most of the device structural parameters. The key element in the VFET architecture is the source electrode structure, sandwiched between the gate and gate dielectric layers, on one side, and the active layer and drain electrode, on the other.

In 2004, Yang and coworkers have demonstrated a high performance device realized with an ultra-thin Al electrode, stacked upon a high roughness dielectric layer, serving as the source electrode.[8] The effect is explained in Ref. 8 as follows: charge accumulation on the source/active-layer interface determined by the Debye shielding length sets the charge injection performance. In addition to having non-uniform thickness and partially oxidized composition, the short Debye shielding length requires the gate dielectric to be a super high capacitor, above 1 μF/cm^2, limiting the device frequency performance. This approach was recently combined with the enhanced electric eouble layer (EDL) gate dielectric.[9] Porous SiO_2 fabricated by plasma enhanced chemical vapor deposition under certain conditions results in capacitance greater than 1 μF/cm^2.[10] For the sake of comparison, thermally grown 150 nm SiO_2 layer has a capacitance of 20nF/cm^2. Such structures can outperform lateral organic TFTs in terms of low voltage and high current density but are also inherently limited to low frequency as the EDL dielectric is an ion-based capacitor.[11] A different approach for pure VFETs does not consider the source Debye shielding length but instead the source spatial structure which includes perforations, resulting in a planar metal grid structure (patterned electrode).[12,13] The patterned electrode geometrical structure lessens the source electrode screening effect, hence, super capacitance is not required and the theoretical frequency limit is dramatically reduced. The patterned electrode can take forms other than a metallic grid. Porous electrode spin coated from a dilute solution of single wall carbon nano tubes[14–16] results in a conductive network that serves as a conductive porous layer. Lately, we have presented a facile fabrication

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method which results in a metallic Patterned Electrode Vertical OFET (PE-VOFET) with perforations determined in size and shape,[12] yielding a complex electrode structure. PE-VOFET is realized through patterning of the source electrode, using polystyrene poly(methyl-methacrylate) block-copolymer (BCP) self-assembled layer.[17] The source patterning process, obtained by transferring the BCP pattern to the metal electrode, offers accurate control of the source composition, architecture and dimensions. The freedom to select any conductive source materials allows the fabrication of either n-type or p-type transistors with various active layer materials. In addition, fabrication of architecture with different structural dimensions opens the route for comprehensive investigation of the device operation and its optimization.

The current work aims to present a comprehensive view of the PE-VFET performance, based on numerical analysis. Experimental measurements are presented to support the simulation results. In Sec. II we describe the device architecture and the structure we use for the simulation analysis. The physical model and the method of its implementation are specified in Sec. III. Based on the numerical analysis, Sec. IV sheds light on the physical processes affecting the device operation and presents analytical description for the device operation at On and Off states which are supported by experimental data. Section V attempts to clarify the influence of the different structural parameters on device performance and provides structural optimization guidelines.

II. DEVICE DESCRIPTION

Similar to a lateral FET, the vertical type also includes a dielectric layer sandwiched between the gate electrode and the active layer. However, in the VFET the active layer is sandwiched also between the source and the drain electrodes. The device structure comprises of five layers stacked one upon the other: The bottom gate which could be highly doped silicon wafer, the dielectric layer (as thermally grown oxide layer), the source electrode (SE) with the grid shaped metallic structure, the semi conductive (active) layer, and the drain as the top electrode. The device ideal structure presented in Fig. 1(a) shows a SE layer having a periodic structure with identical circular shaped perforations. This structure is somewhat justified by the fabrication method based on BCP self-assembly[18] which determines the perforations size and shape.

In this paper, we will use the following definitions for the structural parameters. The distance between the source and drain electrodes determined by the active layer thickness defines the channel length, L. The vertical FET area, A, is determined by the overlap between the gate, source, and drain electrodes. D is defined as the perforation diameter, and the Fill Factor value, FF, is defined as the ratio between the sum of the perforations area to A. h_d and h_s are the dielectric thickness and the SE thickness, respectively. Finally, the contacts potential, φ_{b0}, is defined as the difference between the electrodes work functions and the active layer LUMO/HOMO levels. Figure 1(b) presents a 2D cross section utilized by the numerical simulation. The cross section provides a side view of the device single active cell as indicated on Fig. 1(a). The active cell is spatially comprised of a single perforation surrounded by the metallic source layer and extends vertically to include all the layers.

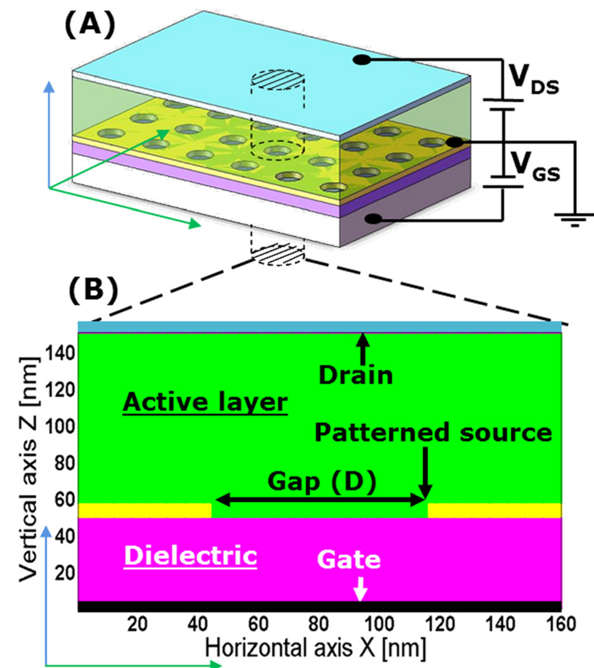

FIG. 1. (Color online) Description of device architecture. (a) Illustration of vertical 3D device ideal structure with a cylindrical active cell. (b) Simulation 2D cross section of the device active cell with the layers notations.

III. MODEL DESCRIPTION

A. Physical picture

Having the explicit description of the device geometrical structure, we now provide the physical picture within which we describe the device operation. The model takes into account drift and diffusion of charge carriers and the effect of space charge on the electric field in the device. Unique properties of organic semiconductors are not accounted for in the present model; among these are the generalized Einstein relation[19] and the field dependent mobility.[20] The basic equations used for the simulation are described below. Equation (1) is the 2D Poisson equation relating the potential shape to the device geometrical structure, through the boundary conditions, and to the charge density distribution

$$\left[\frac{\partial^2\psi(x,z)}{\partial x^2}+\frac{\partial^2\psi(x,z)}{\partial z^2}\right]=\frac{q}{\varepsilon(x,z)\varepsilon_0}[n(x,z)-p(x,z)], \quad (1)$$

where q, ε, and ε_0 are the elementary charge, the vacuum permittivity and the relative permittivity, respectively. n and p are the electron and hole density values. For the sake of convenience, the spatial notations are dropped in the following sets of equations. Charge conservation is applied through the current continuity equations [Eq. (2)] for electrons and holes

$$\begin{cases}(a)\ div\overrightarrow{J}_n - q\dfrac{\partial n}{\partial t}=qR,\\ (b)\ div\overrightarrow{J}_p + q\dfrac{\partial p}{\partial t}=-qR,\end{cases} \quad (2)$$

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where J_n, J_p, and R are the electrons current density, the holes current density, and the recombination rate, respectively. Equation (3) are the drift diffusion equations for electrons and holes describing the relation between the current density and both the charge distribution and the potential shape

$$\begin{cases}(a)\overrightarrow{J}_n = qn\mu_n\overrightarrow{E}_n + qD_n grad(n),\\(b)\overrightarrow{J}_p = qp\mu_p\overrightarrow{E}_p - qD_p grad(p),\end{cases} \tag{3}$$

where μ_n, μ_p, D_n, and D_p are the mobility and diffusion coefficients for electrons and holes, respectively. The ratio between the diffusion and mobility is taken to be given by the classical Einstein relation $D_i/\mu_i = k_BT/q$, where k_B and T are the Boltzmann constant and the temperature, respectively. Using Eq. (3) and assuming steady state conditions ($\partial n/\partial t = 0$ and $\partial p/\partial t = 0$) and zero generation/recombination, Eq. (2) are reduced to

$$\begin{cases}(a)\dfrac{\partial}{\partial x}\left(-n\mu_n\dfrac{\partial\psi}{\partial x}+D_n\dfrac{\partial n}{\partial x}\right)+\dfrac{\partial}{\partial z}\left(-n\mu_n\dfrac{\partial\psi}{\partial z}+D_n\dfrac{\partial n}{\partial z}\right)=0,\\(b)\dfrac{\partial}{\partial x}\left(n\mu_p\dfrac{\partial\psi}{\partial x}+D_p\dfrac{\partial p}{\partial x}\right)+\dfrac{\partial}{\partial z}\left(p\mu_p\dfrac{\partial\psi}{\partial z}+D_p\dfrac{\partial p}{\partial z}\right)=0.\end{cases} \tag{4}$$

B. Boundary conditions

Obtaining a unique solution using the set of differential Eqs. (1) and (4) requires the carriers density and the potential value to be specified at the boundaries. For the device structure used, the potential shape is solved for the entire device but the carriers density distributions are solved solely in the active layer, introducing boundary conditions spatially located interior to the device. These boundary conditions are located at the interfaces between the active layer and the source/drain electrodes and the dielectric layer, at the bottom of the perforation. The boundary conditions at the electrodes determine the potential value on their surface through the applied bias (V_G, V_D, and $V_S = 0$) and the contact potential, φ_{b0}, between each electrode and the active layer. We considered the electrodes to have infinitely short Debye length and hence fixed work function value regardless of the applied electric field. The electrons/holes charge density in the interface is assumed to be in equilibrium with the electrodes,[21]

$$n = N_0\exp\left(-\frac{q\varphi_b}{k_BT}\right), \tag{5}$$

where N_0 is the density of states in the active layer. φ_b is the energetic potential barrier determined by

$$\varphi_b = \varphi_{b0} - \Delta\varphi = \varphi_{b0} - \Delta x E_{\perp}, \tag{6}$$

where $E_{\perp}$ is the electric field perpendicular to the interface and Δx is the distance between the metal surface to the first site at the active layer (taken to be the intermolecular spacing of ~1 nm, the mesh increment in the simulation). We note that the image potential influence here, obtained through the solution of the 2D Poisson equation in the vicinity of the electrodes BCs, is only partially considered. The solution, being based on charge densities substantially, lessens the image potential magnitude rendering the phenomena insignificant. Furthermore, the commonly used formula for the image potential[21–23] was developed for the case of a charge next to an infinite metal plane. This case is very different than the scenario at the perforations (gap) where the metal surface extends vertically only few nm, a case in which the influence of the image potential is reduced in size.[24] The boundary conditions at the sides ($x = 0$ and $x = 160$ nm in Fig. 1) are described by cyclic boundary conditions. The insulating interface between the dielectric layer and the active layer, at the bottom of the perforation, is assumed to be free of surface charges and with zero vertical current.

C. Numerical method and parameters

The model assumes initial condition of charge neutrality to implicitly obtain the potential shape [Eq. (1)]. The implicit solution of Eqs. (4a) and (4b) incorporates the Scharfetter-Gummel method.[25] The method calculates the current values in the middle of each mesh interval under the approximations that electric field, mobility, and diffusion coefficients are fixed in the entire interval. The electrons and holes currents at a mid-interval point along the x axis are

$$\begin{cases}(a)\ J_{n,i+\frac{1}{2},j} = \dfrac{qD_n}{\Delta h}\left[B(^xt_i)n_{i+1,j} - B(-^xt_i)n_{i,j}\right],\\(b)\ J_{p,i+\frac{1}{2},j} = \dfrac{qD_p}{\Delta h}\left[-B(^xt_i)p_{i+1,j} + B(-^xt_i)p_{i,j}\right],\end{cases} \tag{7}$$

where i and j are the calculation point indices along the x and z axis, respectively, Δh is the interval length, B is the Bernoulli function $B(t) = t/(e^t - 1)$ and ^xt_i is given by $^xt_i = (\mu_n E^x_{i+1/2,j}\Delta h)/D_n$ (where x denotes the measured field direction).

Convergence to the steady state solution is obtained using iterative method.[26] The iteration solves first the continuity equation with damping factor to ensure numerical stability, then the Poisson equation is solved, and finally the boundary conditions are updated.[27] The finite element method is realized using fixed mesh increments of 1 nm to both the x and z axis, similar to the molecular distance of crystalline fullerene, the material of choice for the active layer of the reference measured devices.[28] The shape and location of the different layers is presented in Fig. 1(b). The typical dimensions used for the following investigation are $h_d = 50$ nm, $h_s = 5$ nm, $L = 100$ nm, $X_{width} = 160$ nm, $D = 60$ nm, $FF = D/X_{width} = 37.5\%$, and $\varphi_{b0} = 0.6$ eV (the barrier between the source and the active layer LUMO level). Single carrier type is assumed and we solve only for electrons (will be justified in Sec. IVA).

IV. OPERATION DESCRIPTION

In this section, we use the numerical simulations to produce the distribution of the various quantities (charge carrier density, potential, and current) and to provide some insight and understanding of the operation of such vertical FET structure.

A. Potential surface

As was briefly described in Ref. 12, the device operation relies on the gate potential inducing electric fields which pull

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the charges out of the SE and into the perforation area (i.e., gap) such that a virtual contact is created. To understand the device operation in more detail, one has first to follow the potential lines in such a device and their dependence on the structural parameters. We first consider the device without any injected charges present. In a non-patterned source configuration, the potential shape would have been very simple, comprising two flat surfaces, one between the gate and the source, and the other between the source and the drain (dashed line in Fig. 2). When the source electrode is completely removed only one flat surface exists between the gate and the drain (dotted line in Fig. 2). The perforated electrode shape is a mix of both cases, resulting in a complex potential surface. The solid line in Fig. 2 shows the potential spatially located at the perforation center and along the vertical axis. The difference between the dotted and solid lines indicates the existence of lateral electric fields concentrated at the area of the perforations. The arrow in Fig. 2 indicates the point at which the electric field, at the center of the gap, changes sign and starts to pull electrons toward the drain electrode. We term this point as "inversion point" and as we will show, its position is affected by the source electrode thickness and it influences device performance. We elaborate on the inversion point in Sec. IV B.

The shape of the potential surface with the same biasing conditions as in Fig. 2 solved by the numerical simulation is presented in Fig. 3(a). Figure 3(a) shows that for the vertical configuration the gate effect is restricted to the close proximity of the source perforations and specifically it does not affect the drain electrode injection properties. Therefore, injection through the drain would contribute only to the device leakage current and hence, its injection properties have to be minimized through judicious choice of the electrode material. The above leads to the conclusion that an optimized vertical device is of single carrier type, as considered in the numerical model.

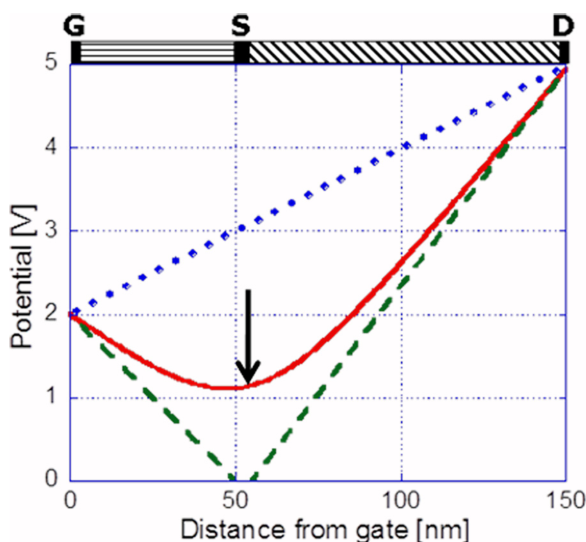

FIG. 2. (Color online) Schematic description of the potential distribution in a device empty of charges with $V_G = 2$ V, $V_S = 0$ V, $V_D = 5$ V. Dotted line represents a structure with the SE removed. Solid line represents a structure with a gap size of 60 nm and SE thickness of 5 nm (vertical arrow denotes the point at which the electric fields start to pull electrons toward the drain). Dashed line represents the potential outside the perforated region.

The electric fields quiver plot shown in Fig. 3(b) demonstrates the electric field magnitude and direction in the region close to the perforation edge. We distinguish between the side and upper interfaces of the SE with the active layer and refer to them as the source lateral facets and the source top facet, respectively. Modifying the gate potential, non-homogeneously varies the electric field applied to the SE surfaces. Examining the electric field values close to the interface we find that the maximum increase in the electric field is at the bottom of the lateral facets and it lessens as one moves away from the dielectric surface. Furthermore, the electric field over the source top facet is negligibly affected by the gate, indicating that the gate's main role is in varying the injection properties of the source lateral facets. More insight is gained through analytical Laplace model developed based on the numerical simulation results (see the Appendix). As is shown in the Appendix, most of the charge injection (extraction from the SE) at the On state takes place at the bottom of the perforations' lateral facets in close proximity to the dielectric surface.

B. Charge carrier concentration

Charge carrier concentrations are presented in Fig. 4. Simulation results are obtained for a device with the same structural parameters as in Fig. 4 and for biasing conditions of $V_G = 5$ V, $V_D = 2$ V, and $V_S = 0$ V. Figure 4 omits the gate electrode and gate dielectric layers as they do not participate in charge carrier conduction. The charge extracted from the

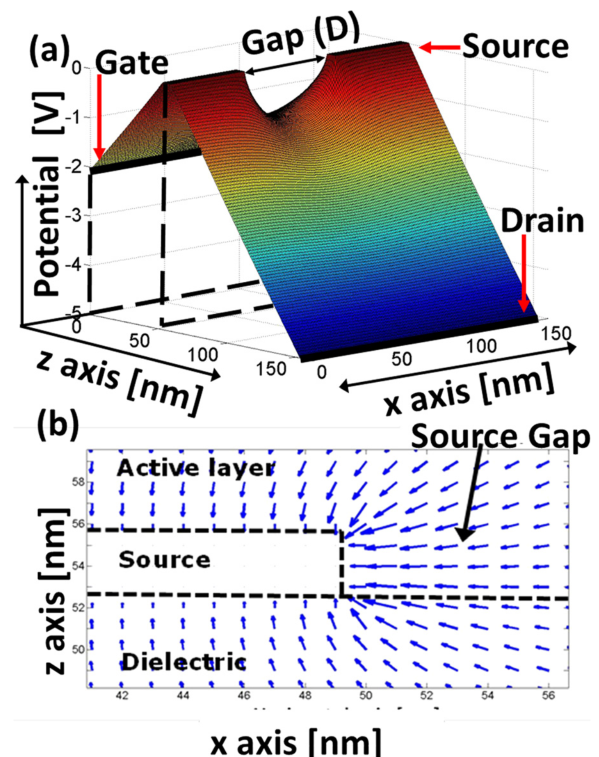

FIG. 3. (Color online) (a) Potential surface shape in an active device with structural parameters of $D = 60$ nm, $FF = 37.5\%$, $h_d = 50$ nm, $h_s = 6$ nm, $\varphi_{b0} = 0.6$ eV, and $L = 100$ nm, and biasing conditions: $V_G = 2$ V, $V_S = 0$ V, $V_D = 5$ V. The vertical white arrow denotes the point at which the electric field, at the center of the gap, starts to pull electrons toward the drain. (b) Electric field quiver plot focused on the area of the gap edge.

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lateral perforation facets by the lateral electric fields accumulates within the perforation at the dielectric interface, forming the virtual contact which is the origin of the vertical channel. Figure 4 shows that indeed the vertical channel is located above the source perforation. The experienced reader may note that the shape of the charge density resembles that found in space charge limited diode. We will revisit this observation later in the text.

1. The inversion point

The details of the shape of the vertical channel do not depend only on the fields within the perforation but also on the vertical electric fields in the active layer and particularly above the perforation area. Unlike the lateral electric fields, the vertical ones projected by the gate and drain electrodes are opposite in direction. This effect led to the convex shaped potential line along the device vertical axis (Fig. 2, solid line), indicating that the vertical electric fields direction switches along this line. The spatial location of this turning point which we refer to as the inversion point is a function of the device structural parameters and the biasing conditions.

Determining the inversion point spatial location and its potential cannot be done analytically with Laplace interpretation as the high charge accumulation significantly alters the shape of the potential at the vertical channel area. The vertical electric fields between the insulator surface, the origin of the accumulation, and the inversion point are in direction opposite to that applied by the drain. Therefore, the charge concentration at the inversion point is actually driving the rest (upper part) of the vertical channel. The spatial distance and the related potential difference between the dielectric layer and the inversion point determine the charge density at that point with the potential difference acting as an effective barrier. Namely, the properties of the inversion point (location/potential) affect the resulting current density where a shorter distance would imply higher current.

C. Current flow

As the influence of the gate over the source electrode top facet is negligible the varying charge injection attributed to the On current would occur solely at the gap from the source lateral facets. As the charge that accumulates in the gap can flow only in the vertical direction one would expect a vertical channel to extend from the gap to the drain electrode (see Fig. 4). In this scenario one can separate the device into two different functional regions. The region between the dielectric (in the gap) and the drain can be referred to as the On region (the channel) while the region above the SE top facet can be referred to as the Off (or "leakage") region.

The device current density quiver plot, at active state (after channel formation), is shown in Fig. 5. The arrows denoting the current are overlaid on top of the charge concentration contour (shown in Fig. 4) for better orientation. Direction of electrons flow is indicated with arrows, the length of which is logarithmically scaled with the current density (note that the vertical and horizontal axes are not to scale). The carriers' path is initially in horizontal direction from the gap edges to the gap center. Its density is at its maximum in close proximity to the dielectric interface and reduces fast as the distance from the dielectric layer increases. The current then turns to the vertical direction, driven initially by diffusion forces and kept at the center of the perforation due to the lateral electric fields exerted by the perforation facets. As Fig. 5 shows, the current initially flows through a very short "tunnel" the length of which is determined by the SE thickness. The effect of this "tunnel" will be discussed later in the text.

D. Channel width (*W*)

It is common to associate the channel width with the length of the injecting contacts. In the PE-VFET architecture, the channel width would thus be measured by summing the length of all the SE lateral facets. This value could be assessed analytically assuming the perforation (gap) takes either ideal circular or striped shape

$$\begin{cases} (a)\ W_{\text{interface-striped}} = \dfrac{2FF \times A}{D}, \\ (b)\ W_{\text{interface-circular}} = \dfrac{4FF \times A}{D}. \end{cases} \tag{8}$$

Using the previously mentioned BCP fabrication method the perforation diameter is roughly 60 nm and the *FF* is around

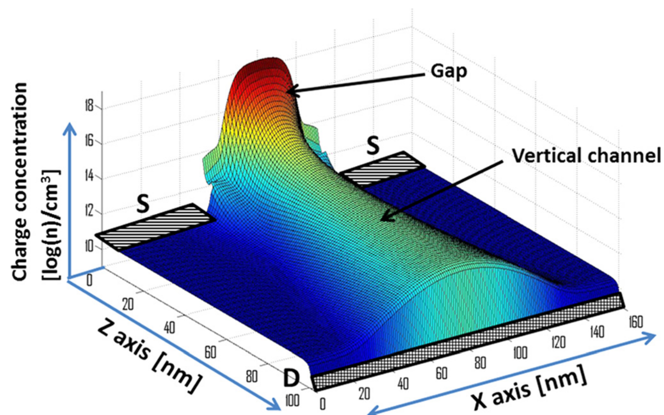

FIG. 4. (Color online) Charge concentration distribution, logarithmic scale, for a device with structural parameters of $D = 60$ nm, $FF = 37.5\%$, $h_d = 50$ nm, $h_s = 6$ nm, $\varphi_{b0} = 0.6$ eV. and $L = 100$ nm, and biasing conditions: $V_G = 5$ V, $V_S = 0$ V, $V_D = 2$ V.

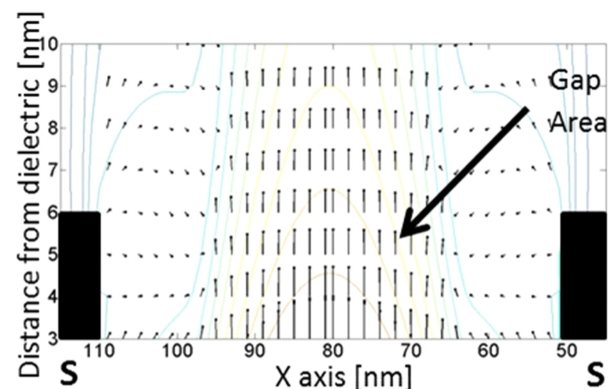

FIG. 5. (Color online) Current density quiver plot overlaid on top of the charge concentration contour for a device with structural parameters similar to those in Fig. 4 and biasing conditions: $V_G = 3$ V, $V_S = 0$ V, $V_D = 2$ V. Arrow size is logarithmically scaled with the current density.

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30%. For a device in total area of 10 mm^2, the channel width value is between 100 to 200 m according to Eqs. (8a) and (8b), respectively. For the sake of comparison, lateral devices fabricated with lithographic resolution of 1 μm occupying the same surface area have approximately 3 mm channel width, five orders of magnitude smaller. The large channel width at the vertical device indicates that these interfaces would not constitute a bottleneck for the current-voltage behavior in the active state.

E. On and Off states

General device behavior can be deduced using the following three observations: First, the On current originates only from the perforations area. Second, the Off current originates solely from the rest of the SE (i.e., top surface). Third, the channel width is large and hence does not constitute a bottleneck for the current voltage behavior in active state. Following the above observations we consider two limiting cases for the current regimes. In the first limiting case, when the device is at Off state, charges are extracted to the active layer only due to applied drain-source voltage. In this configuration the similarity to a diode structure is obvious and we expect Contact Limited (CL) behavior which is described by Eq. (9),

$$J_{\rm Off} = q\mu_n N_0 E_\perp \exp\left(-\frac{q\varphi_b}{kT}\right)(1-FF), \qquad (9)$$

$E_\perp$ is the perpendicular electric field applied to the SE top facet, $L_{\rm Off}$ is the Off Channel length (the distance between the SE top facet and the drain electrode), and the (1-FF) factor accounts for the Off current originating from only part of the device area (SE top surface). The second limiting case occurs when the device is at the On state and charges are extracted from the source electrode by the gate and accumulate at the perforations. The large accumulation of charges at the dielectric interface in the source perforations creates the virtual contact and if the density is sufficiently high it will act as an "infinite" charge reservoir as would be the case for an ohmic contact. In that case, space charge limited current (SCLC) regime is expected where the device behaves according to Eq. (10)[20,21,29] and the (FF) factor accounts for the On current originating only from the perforations area.

$$J_{\rm On} = \frac{9}{8}\varepsilon_0\varepsilon\mu_n\frac{V_{DS}^2}{L^3}FF. \qquad (10)$$

These two limiting cases are best observed when measuring the device output characteristics, sweeping the drain potential while the gate is either closed (Off state = gate source bias is negative with respect to the drain source bias) or fully open ($|V_{GS}| \gg |V_{DS}|$). To illustrate the strength of these observations we show below a parameter extraction procedure applied to a measured PE-VFET device. We note that the Gate potential values at the experimental part ($V_G = 40$ V) are higher than those in the theoretical part ($V_G \leq 10$ V) primarily due to geometrical differences. In this context, the most relevant feature is the dielectric thickness which is equal to 100 nm in the experimental part and 50 nm in the theoretical part (see Fig. 14).

Output curves of measured devices at On and Off states are shown in Fig. 6(a) and Fig. 6(b) (circles), respectively. Curve fitting at On state (SCL regime) based on Eq. (10) is shown in Fig. 6(a) (solid line). The curve fitting for contact limited regime (Off state) based on Eq. (9) is shown in Fig. 6(b) (solid line). For this fit, shown in Eq. (12), we use the image force barrier lowering described in Eq. (11).[23]

$$\varphi_b = \varphi_{b0} - \Delta\varphi = \varphi_{b0} - \sqrt{\frac{qE_\perp}{4\pi\varepsilon_0\varepsilon}}, \qquad (11)$$

$$J_{\rm Off} = q\mu_n N_0 \exp\left[-\frac{q}{kT}\left(\varphi_{b0} - \sqrt{\frac{qV_{DS}}{4\pi\varepsilon_0\varepsilon L_{\rm Off}}}\right)\right] \times \frac{V_{DS}}{L_{\rm Off}}(1-FF). \qquad (12)$$

We use $E_\perp = [V_{DS}/L_{\rm Off}]$ assuming that in the regions outside the perforation area, between the source and the drain, the electric field is constant due to low charge concentration at CL regime.

Fitting coefficients values extracted from the device characteristics shown in Fig. 6 are detailed in Table I, where the first two coefficients are ascribed to the Off state measurement and the third coefficient is ascribed to the On state measurement.

Device parameters (detailed in Table II) are then determined as follows. Effective channel length is determined first through coefficient #2, mobility is determined through coefficient #3 and potential barrier is determined through coefficient #1 (we assume the mobility at CL and SCL regimes is unchanged and $L \approx L_{\rm Off}$).

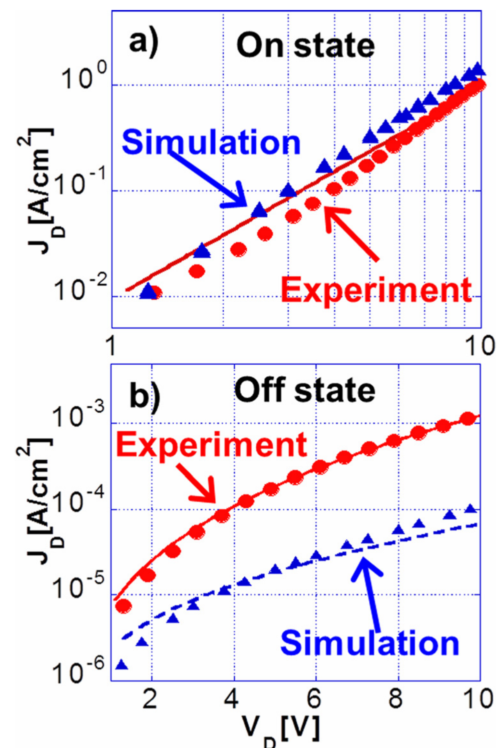

FIG. 6. (Color online) Output characteristics for experimental measurements (circles) and simulation results (triangles). Fitting curves indicated with solid lines. (a) Device at On state, $V_G = 40$ V. (b) Device at Off state, $V_G = -5$V. Dashed line is the calculated curve based on Eq. (9) for a device with no potential barrier lowering due to image potential.

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TABLE I. Experimental fitting parameters describing the CL and the SCL regimes obtained based on Eqs. (10) and (12).

	(#)	Parameter	Exp. fit
CL	(1)	$q\mu_n N_0(1\text{-}FF)/L_{Off}$X Exp$[-q\ \varphi_{bo}/(kT)]$	1.99×10^{-6}
	(2)	$q/(kT)$X$(q/(4\pi\varepsilon\varepsilon_0 L_{Off}))^{0.5}$	1.306
SCL	(3)	$9/8$X$\varepsilon\varepsilon_0\mu_n FF/L^3$	9.5×10^{-3}

We note that L_{eff} is found to be smaller than the nominal evaporated layer thickness and we attribute it to the film surface morphology characterized with irregular stacking of crystal grains formed when C_{60} film is grown on various surfaces even at room temperature.[30] We also note that the *FF* parameter is evaluated prior to device fabrication based on Atomic Force Microscopy measurement by summing up the perforations area at the SE. However, the effective *FF* value is smaller than the "physical" one due to the "tunnel" effect rendering only part of the perforation area active. The difference between the effective and "physical" *FF* was demonstrated using the simulation (not shown here) and its size is a factor of structural parameters, i.e., perforation height and diameter. In the above applied parameter extraction procedure, the error associated with the *FF* value was not taken into consideration hence the mobility value extracted based on coefficient #3 is underestimated.

Using the parameters detailed in Table II we performed a simulation run, the results of which are presented in Fig. 6 (triangles). The output characteristics describing the On state [Fig. 6(a)] are similar to the measured device's ones; however, at Off state [Fig. 6(b)] the simulation predicts lower current density than measured experimentally. This deviation mainly originates from the lack of the image potential barrier lowering not accounted for in the simulation. The dashed line in Fig. 6(b) is a calculation of Eq. (9), using Eq. (6) for the barrier height, based on the parameters described in Table II. This calculation shows that indeed the deviation at the Off state between the simulation and the measured data is largely due to the exclusion of the image force barrier lowering at the top surface of the source electrode.

V. ROLE OF STRUCTURAL PARAMETERS

The following section analyzes the coupling between structural parameters and device performance. The analysis is performed with numerical tools and provides more accurate understanding regarding device behavior as well as structural optimization tools. Structural features are investigated one by one focusing mainly on parameters unique to the PE-VFET architecture. Device performance is analyzed in the context of On/Off current ratio, output current, threshold voltage and Subthreshold Swing (SS). We note that for disordered organic transistor operating in accumulation regime, the threshold voltage serves as a fitting parameter[31,32] associated with the formation of the virtual contact.

TABLE II. Experimental parameters obtained for PE-VOFET with fullerene (C_{60}) active layer.

Parameter	Value
μ_n[cm^2/Vs]	1.7×10^{-3}[a]
N_0[cm^{-3}]	1.44×10^{21}[c]
T[°K]	300
L_{eff}[nm]	315[a]
φ_{b0}[eV]	0.57[a]
FF	0.45[b]
ε	4[c]

[a]Extracted from the fitting coefficients at Table I.
[b]Atomic force microscopy measurement prior to device fabrication.
[c] Based on literature.[28]

A. Source electrode thickness

Figure 7(a) shows the transfer characteristics of simulated devices with source electrode thickness (h_s) varying between 2 to 50 nm. Other structural parameters are kept constant and are the same as those of the previous section. Specifically, the distance between the SE top surface and the drain electrode is kept constant and hence the current density at zero gate bias remains constant. As Fig. 7(a) shows, increasing the source electrode thickness leads to performance degradation: SS value increases from 1.3 V/decade for 2 nm thick SE to 4.8 V/decade for 50 nm thick SE; threshold voltage increases; On/Off ratio, measured at $V_G = 10$ V and $V_G = 0$ V, reduces by three orders of magnitudes along with the On current output. Figure 7(b) shows the On/Off ratio as a function of h_s and we note the functional form is close to exponential. Deviation from the exponential dependence occurs for ultra-thin ($h_s < 5$ nm) and relatively thick ($h_s > 40$ nm) SE. This behavior can be explained by examining the role of h_s in determining the properties of the inversion point (location/potential) relative to those at the insulator interface which is the On channel origin.

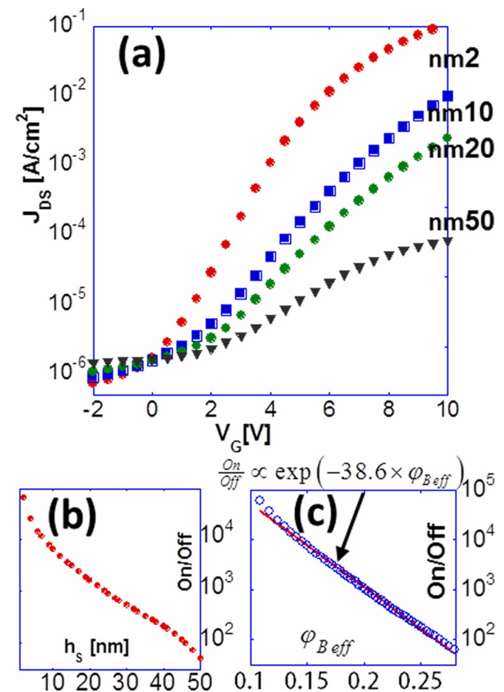

FIG. 7. (Color online) (a) Transfer characteristics of devices with varying h_s values and fixed Off channel length (100 nm) with $V_D = 3$ V. (b) On/Off ratio vs SE thickness. (c) On/Off ratio vs potential barrier height at the inversion point.

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The simulations show that as h_s increases, the distance between the inversion point and the dielectric interface also increases. Actually, if we plot Fig. 7(b) as a function of the distance between the inversion point and the dielectric interface, instead of the SE thickness, the exponential relation is even more pronounced (not shown here). This observation led us to plot at Fig. 7(c) the On/Off ratio as a function of the potential difference between the inversion point at the center of the perforation and the dielectric interface (φ_{Beff}). The almost perfect exponential fit indicates that the inversion point displays an effective potential barrier to charge injection from the virtual contact into the upper part of the vertical channel. This observation, along with the results shown in Fig. 5, indicate that the charge flow between the dielectric interface and the inversion point is, to a good approximation, one dimensional.

We conclude that the device operational mechanism includes two barriers. The first, between the SE and the active layer (contacts barrier), is determined by the choice of materials and is either gate-controlled at the lateral facets or drain-controlled at the top facet. The second, the inversion point barrier, is located inside the active layer.

1. The inversion point and the tunnel effect

One of the implications of the inversion point is that at this point the diffusion-controlled current flowing toward the drain becomes drift-controlled. As can be seen in Ref. 33, Fig. 6(b), this situation is found in every space charge limited device. The other effect illustrated in the same paper [Fig. 6(a)] is that the charge density drops exponentially between the contact and the point at which the electric field changes sign. In a standard SCLC diode the position of the inversion point would depend largely on the charge density at the contact interface, which in our case translates to the charge density accumulated at the dielectric interface (the virtual contact), and slightly also on the diode bias. In the current structure, however, the current starts its flow between two source facets (see Fig. 5) which are of constant potential (generally zero). Such a "tunnel" with equipotential walls acts to prevent the electric field at the vicinity of the walls from changing sign before the "tunnel" ends. Closer to the center of the gap ("tunnel"), the effect would be weaker but still the inversion point would move toward the drain as the thickness of the source electrode increases. Since the charge density would decay exponentially toward the inversion point, the farther the inversion point, the lower the density that is supplied to the upper part of the channel that is governed by the drift current. As mentioned above, the effect of the inversion point position on the device performance (On current and On/Off ratio) is very strong [Fig. 7(b)]. Namely, due to the "tunnel" effect it is important that the source electrode is thin enough (<5 nm) for the device to exhibit best performance.

B. Perforation size and *FF*

In this section, we investigate the role of perforation (gap) size, D, and the FF value by performing three simulation sets:

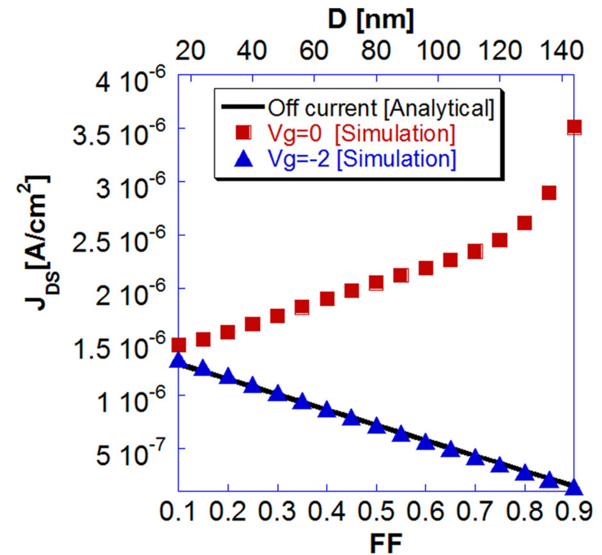

FIG. 8. (Color online) Numerical and analytical Off current density comparison for devices with varying FF or D values. Rectangles: non-biased gate. Triangles: reversibly biased gate. Solid line: analytical curve according to Eq. (9).

1. The unit cell length, X_{width}, is kept constant and D is varied (FF changes accordingly and in the 2D simulation it means: $FF = D/X_{width}$);
2. The perforation size (D) is kept constant and the FF is varied (unit cell length changes accordingly);
3. The FF is kept constant and D is varied (unit cell length changes accordingly).

In set #1 (Figs. 8 and 9), D and FF are linearly proportional while the device unit cell size is constant ($X_{width} = 160$ nm as in Fig. 1). The FF value varies between 0.1 and 0.9 together with the gap size (D) which varies accordingly, between 16 and 144 nm. Figure 8 shows the current density for devices biased at $V_{DS} = 2$ V and $V_{GS} = 0$ V (rectangles) or $V_{GS} = -2$ V (triangles) as a function of the FF (or D) value. As was discussed earlier, the current flowing from the source may originate either from the lateral facets of the perforations or from the top surface of the electrode. As the FF increases, the area of the top surface decreases and hence the increase in current for the case where $V_G = 0$ V (rectangles) has to be associated with the lateral facets. Close examination of the simulation outputs reveals that there is a more effective barrier lowering at the lateral facets for larger D values. The lower curve for $V_G = -2$V (triangles) decreases linearly, indicating that the reverse-biased gate electrode eliminates the current flow from the lateral facets, leaving only the top surface as the origin for charges. Therefore, in this device configuration, measurements of drain-source leakage currents, as described in Eq. (9), are obtained only when the gate is oppositely biased to the drain electrode (Fig. 8, solid line). Under these conditions, when the injection from the lateral facets (into the gap) is completely suppressed, the Off current originates solely from the SE top facet. The Off current value decreases linearly with FF value (triangles) and is linearly proportional to the top surface area.

Transfer characteristics of the same set are shown in Fig. 9 and exhibit a strong dependence on FF and D values. Varying the gap size (D) and the FF results with On/Off ratio

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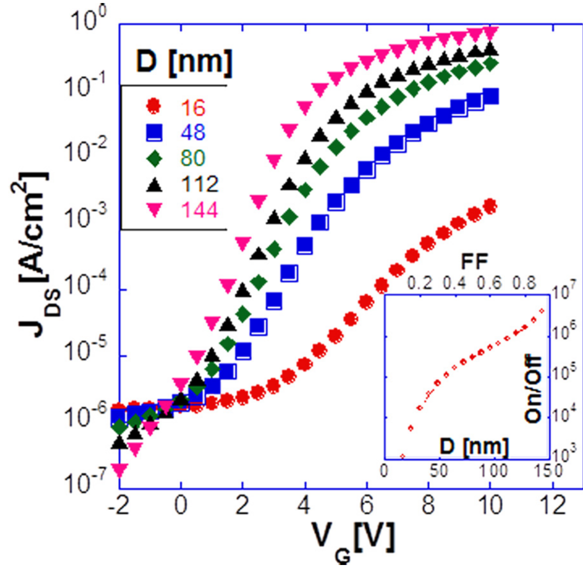

FIG. 9. (Color online) Transfer characteristics for devices with varying $FF(D)$ values. Inset: On/Off performance as a function of $FF(D)$ value.

increased by over three orders of magnitude with the On current taken at $V_G = 10$ V and the Off current at $V_G = -2$ V. The SS varies between 3.2 V/decade for $D = 16$ nm to 1.3 V/decade for $D = 144$ nm. The inset to Fig. 9 presents the On/Off performance as a function of D (FF). Examining this inset together with Fig. 7(b), the effect can be intuitively explained by referring to the perforation relative dimensions or the "tunnel" effect. Thicker electrode and smaller gap size result in a more pronounced "tunnel" structure which reduces the device performance, and vice versa (see discussions in Secs. V A 1 and IV B 1).

Set #2, shown in Fig. 10, is comprised of devices with fixed D and varying unit cell length (X_{width}). Hence, FF values are inversely proportional to the latter. Based on the discussions above, the current at On state originates mainly from the perforation, which in this set is of constant size, and the Off current originates from the top surface of the source electrode. This implies that the relation between the currents at the On or Off states of the devices in this set can be described using purely geometrical factors,

$$\begin{cases} (a)\, J_{\mathrm{On}}(X_{width.1}) = \dfrac{X_{width.2}}{X_{width.1}} J_{\mathrm{On}}(X_{width.2}), \\ (b)\, I_{\mathrm{Off}}(X_{width.1}) = \left(\dfrac{X_{width.2}}{X_{width.2}-D}\right)\left(\dfrac{X_{width.1}-D}{X_{width.1}}\right) I_{\mathrm{Off}}(X_{width.2}), \\ (c)\, \mathrm{On/Off}(X_{width.1}) = \left(\dfrac{X_{width.2}-D}{X_{width.1}-D}\right) \mathrm{On/Off}(X_{width.2}), \end{cases} \tag{13}$$

where X_{width_1} and X_{width_2} are the unit cell length of two different devices. Equation (13a) shows that the current per unit cell is fixed due to the constant perforation size and the current density reduces as the size of the unit cell increases. Equation (13b) shows that due to the increase in the area of the SE top surface, the current density at the Off state will slightly increase. These two equations lead to the On/Off ratio decreasing as a function of the unit cell length (D being fixed and FF decreasing), as indicated by Eq. (13c).

Figure 10 displays a slight increase in the Off current density with unit cell length which is observed at the onset of the transfer characteristics, in agreement with Eqs. (9) and (13b). Similarly a decrease in the On current density with unit cell size is shown as the density of the active sites (FF) is reduced. A complete agreement between the analytical Eq. (13c) and the numerical On/Off performance is shown at the inset to Fig. 10 marked with line and dots, respectively. Note that SS value remains similar for the entire set.

Set #3 is comprised of devices with constant FF value, and D values varying proportionally with unit cell length. Figure 11 presents the transfer characteristics where the onset displays similar Off current density for all devices, validating the constant FF value, according to Eq. (9). The On current, on the other hand, increases approximately linearly with increasing unit cell length (Fig. 11 inset). This increase is proportional to the increase in D, despite the constant value of the FF. This is again due to the "tunnel" effect and the associated barrier discussed previously. For a constant SE thickness the "tunnel" effect would reduce as D increases (see discussion of the inversion point in the context of Figs. 7 and 9).

C. Injection barrier height

As could be deduced from Sec. IV E, the device performance is dependent on the potential barrier height for charge injection from the SE to the active layer (constituting the Schottky barrier). For the following calculations, we use a medium level type of fixed parameters and vary the barrier between the source electrode and the active layer. The fixed parameters are $D = 60$, $X_{width} = 160$, $h_s = 6$, and $h_D = 50$ nm.

Figure 12 shows the transfer characteristics for several injection barrier heights. As expected, the Off current (transfer characteristics at negative gate bias) reduces exponentially with the barrier height. In Sec. IV E, we stated that the On current obtained for $|V_{GS}| \gg |V_{DS}|$ is independent of this injection barrier as the high gate bias would diminish this barrier through the field induced barrier lowering. However,

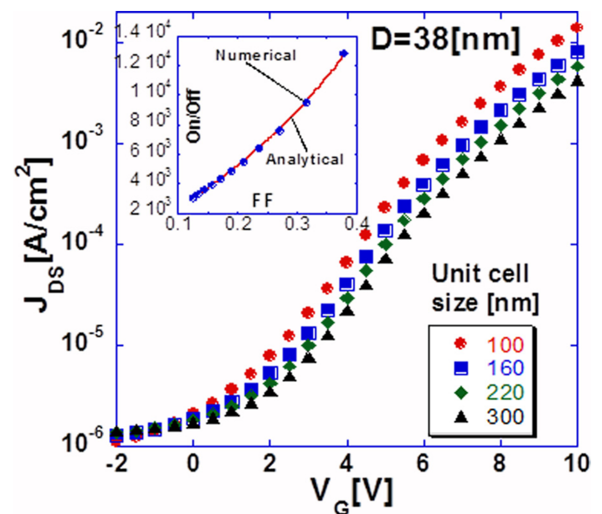

FIG. 10. (Color online) Transfer characteristics for devices with varying unit cell size (X_{width} in Fig. 1(b) and constant D (38 nm). Inset: On/Off ratio vs FF, numerical (dots) and analytical (solid line) evaluations according to [Eq. (13c)], in linear plot.

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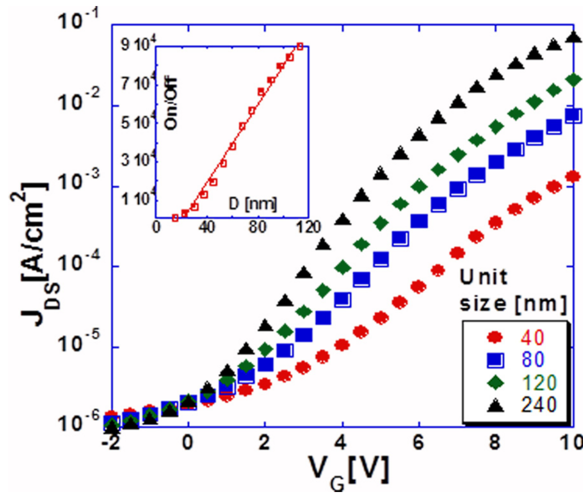

FIG. 11. (Color online) Transfer characteristics for varying unit cell size devices with fixed *FF* value. The inset shows linear dependence between perforation gap size and On/Off performance.

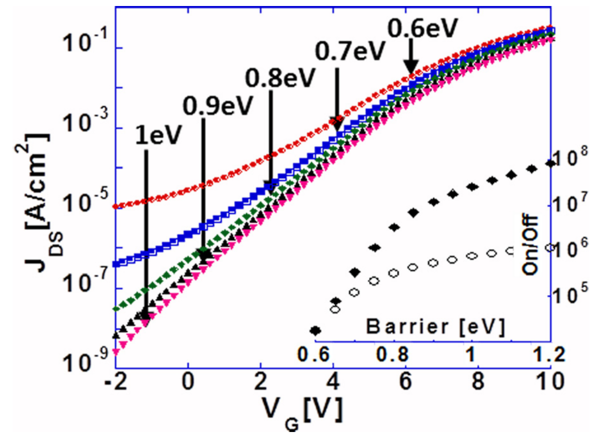

FIG. 13. (Color online) Layered SE devices transfer characteristics with fixed bottom layer potential barrier equal to 0.6 eV and varying potential barrier at the top layer as indicated in the plot. Inset: On/Off performance comparison between the uniform (hollow circles) and non-uniform (full circles) SE structures having the same barrier at their top facet.

Fig. 12 shows that as the barrier increases, the gate bias required to diminish its effect becomes larger. Hence, for the V_G range used in Fig. 12, a full virtual contact is not obtained for the samples with potential barrier of 0.7 eV and above. As a result, in the simulated range, the increase in the On/Off performance (inset in Fig. 12) is accompanied by a reduction in the On current.

To improve the properties of the source electrode one could make use of the fact that the origins of the On and Off channels are spatially separated. This can be manifested if a higher potential barrier is exhibited at the SE top facet (the origin of the Off channel) and a lower potential barrier is presented at the SE lateral facets (the origin of the On channel). Knowing that the On current originated mainly from the bottom of the lateral facet, in proximity to the dielectric interface, allows suggesting a practical solution where the SE would be composed of two layers (i.e., layered structure). The bottom layer provides the lateral facets injection properties and the upper layer provides the top facet injection properties. The transfer characteristics of such devices are presented in Fig. 13. Since Fig. 12 shows that up to about 0.5–0.6 eV the maximum current is not highly affected, we used for the simulations a potential barrier of 0.6 eV for the bottom layer and varied the upper layer potential barrier between 0.6 and 1 eV (see Fig. 13). As anticipated, the Off currents are reduced with increasing top facet potential barrier while the On currents and threshold values remain approximately fixed. The On/Off performance comparison between the uniform (hollow circles) and layered (full circles) SE structures is presented in the inset of Fig. 13 where the potential barrier at the bottom layer is fixed and equal to 0.6 eV and at the upper layer varies between 0.6 to 1.2 eV. Not only is better On/Off performance obtained for the layered structure, but also the On current remains almost unchanged.

D. Dielectric thickness (h_D)

Scaling down of the dielectric thickness (h_D) has the obvious attribute of lowering the gate voltage required to switch the transistor on. The other effect is of reshaping the field lines as the bias is applied across the insulator. In lateral FETs this reshaping through downscaling of the insulator thickness is associated with the gradual channel approximation where optimal performance requires that L (channel length) is

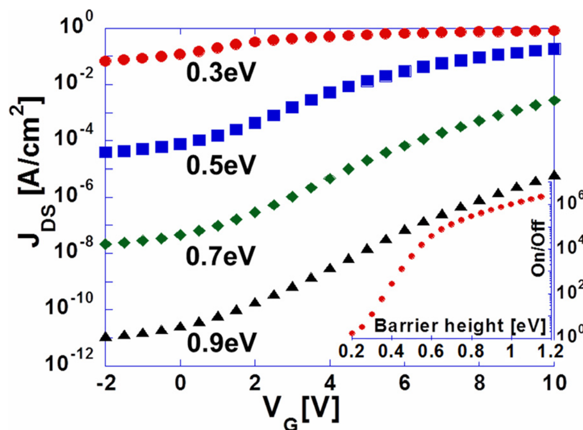

FIG. 12. (Color online) Transfer characteristics for devices with varying SE-active layer potential barrier height. Inset: On/Off performance vs barrier height.

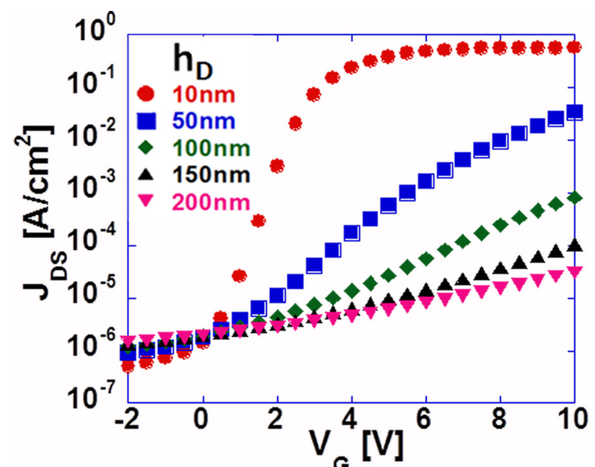

FIG. 14. (Color online) Transfer characteristics for devices with varying h_D.

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at least 1.5 times the length of h_D (i.e., h_D:L ratio of 1:1.5) and, in some cases, 5 times as much.[34,35] The scaling in the case of the vertical transistor configuration is rather associated with the "tunnel" effect discussed earlier. If the "tunnel" effect is the dominant one for this scaling of the dielectric thickness then the ratio to be kept is that of h_D:D. Transfer characteristics presented in Fig. 14 demonstrate the behavior of devices with varying h_D. Comparing the results of Fig. 9 with those presented in Fig. 14, we find that the effect of increasing the perforation size (D) is similar to that of reducing the dielectric thickness (h_D), showing that indeed for a well behaved device the scaling to be considered is of h_D:D and the ratio is to be larger than ~1:3.

VI. SUMMARY

The operation of the PE-VFET was analyzed in the physical framework of semiconductor basic transport equations, realized with a 2D numerical simulation. We have discussed the non-symmetrical VFET structure regarding the source and drain electrodes and the role of the SE architecture in the formation of the virtual contact and, in turn, in the formation of the vertical channel. The device current behavior was shown to follow the SCL- and CL-regimes, with minor modifications [Eqs. (10) and (9)], at On and Off states, respectively. This behavior was theoretically examined versus the 2D simulation and experimentally verified. Under the assumption of zero Debye shielding length, the On channel is formed solely at the SE perforations area and is spatially separated from the Off channel. A series of optimizations and design rules were derived from the simulation and experimental sets. An ideal device requires its SE to be ultra-thin with large perforations (the "tunnel" effect) and with large *FF* value. The device switching performance relies on the SE Schottky barrier; however, its output performance and threshold voltage are negatively influenced. The On and Off channel origins shown to be localized at the SE lateral facets and top facet, respectively, enable a design consisting of two layers shown to provide both high switching performance, similar threshold voltage and similar output performance. While this study centered on PE-VFET architecture with well-defined patterns (based on BCP fabrication methods) the results and especially the physical insights would be applicable also to less ordered fabrication methods such as solution-based nanowire SEs.

ACKNOWLEDGMENTS

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APPENDIX: ANALYTICAL DESCRIPTION OF THE POTENTIAL SHAPE

The potential shape is obtained by solving the 2D homogenous Poisson equation (Laplace problem) in a rectangular space bounded by the gate and the drain electrodes in the vertical direction and by the perforation lateral edges in the lateral direction. Equation (A1) is the Laplace equation form for a rectangular space with normalized variables,

$$\frac{1}{D^2}u + \frac{1}{h^2}u = 0, \qquad \text{(A1)}$$

where D and h are the perforation diameter and the device total thickness, respectively. The boundary conditions (BC) along the upper and lower interfaces are those of equipotential surface and refer to the drain and gate electrodes, respectively. The lateral BCs are symmetrical but more complex, separated into three different regions which represent the potential at the dielectric layer, the source electrode and the active layer. Based on the numerical results a linearly varying potential value is assumed both between the gate and source electrodes and between the source and drain electrodes, as illustrated in Fig. 2 (dashed line). The potential surface is given by Eq. (A2) as an infinite series,

$$u(x,z) = \sum_n \sin(n\pi z)\frac{2}{\sinh\left(\frac{D}{h}n\pi\right)}\left(\frac{1}{n\pi}\right)^2 \times \left\{\left(\frac{V_S - V_G}{h_d}\right)[\sin(n\pi h_d)] - \left(\frac{V_D - V_S}{1 - h_d - h_S}\right) \times \sin[n\pi(h_d + h_s)]\right\}\left\{\sinh\left(\frac{D}{h}n\pi x\right) + \left[\sinh\frac{D}{h}n\pi(1-x)\right]\right\} - [(V_G - V_D)z - V_G], \qquad \text{(A2)}$$

where h_s and h_d are the source electrode and dielectric layer thicknesses normalized by h.

The lateral electric fields [Eq. (A3)] are obtained by deriving the equation of the potential surface over the horizontal axis (x). To simplify, the source electrode potential is grounded and the term for the active layer thickness, h_a, replaces the term (1-h_d-h_s),

$$u_x(x,z) = -\frac{D}{h}\sum_n \sin(n\pi z)\frac{2}{\sinh\left(\frac{D}{h}n\pi\right)}\left(\frac{1}{n\pi}\right) \times \left\{\frac{V_G}{h_d}[\sin(n\pi h_d)] + \frac{V_D}{h_a}\sin(n\pi h_a)\right\} \times \left\{\cosh\left(\frac{D}{h}n\pi x\right) - \cosh\left[\frac{D}{h}n\pi(1-x)\right]\right\}. \qquad \text{(A3)}$$

We require to obtain the electric fields adjacent to the SE lateral facets in order to determine the local potential barrier lowering at the perforations [Eqs. (5) and (6)]. A simpler expression than the one presented in Eq. (A3) is obtained in Eq. (A4) when referring to a specific horizontal location x_0, where x_0 is assumed to be in close proximity to the SE facets ($x_0 \to 0$ or $x_0 \to 1$). For analysis purposes x_0 is considered to be one molecular layer away from the electrode, a distance approximated at 1 nm (the length of one mesh increment in the numerical simulation).

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$$u_x(x_0,z) = \frac{1}{2\pi}\frac{D}{h} \times \left(\begin{array}{l} \frac{V_G}{h_d} \ln\left\{ \frac{1-2e^{-\pi\frac{D}{h}x_0}\cos[\pi(z+h_d)] + e^{-2\frac{D}{h}\pi x_0}}{1-2e^{-\pi\frac{D}{h}x_0}\cos[\pi(z-h_d)] + e^{-2\frac{D}{h}\pi x_0}} \right\} + \\ \frac{V_D}{h_a} \ln\left\{ \frac{1-2e^{-\pi\frac{D}{h}x_0}\cos[\pi(z+h_a)] + e^{-2\pi\frac{D}{h}x_0}}{1-2e^{-\pi\frac{D}{h}x_0}\cos[\pi(z-h_a)] + e^{-2\pi\frac{D}{h}x_0}} \right\} \end{array} \right). \tag{A4}$$

This equation manifests the symmetrical influence of the drain and the gate electrodes, where the equation's first and second parts are ascribed to the gate and the drain, respectively. The electric fields associated with the gate and the drain contributions are both in the same direction but reach their maximum at the bottom and the top of the SE facet, respectively. Both contributions dissipate fast along the vertical axis, ranging from close-to-linear dissipation for extremely thin dielectric ($h_d \approx h_s$), and faster rate of dissipation for thicker dielectric. This behavior indicates that the effective charge injection is a highly localized phenomenon. In a well behaved device the drain influence is minimized so as to minimize the Off currents. In such a case the majority of the charge injection at On state takes place at the bottom of the perforations' lateral facets close to the dielectric surface.

[1]E. D. Mentovich, B. Belgorodsky, I. Kalifa, H. Cohen, and S. Richter, Nano Lett. **9**(4), 1296 (2009).
[2]H. Naruse, S. Naka, and H. Okada, Applied Physics Express **1**(1), 011801 (2008).
[3]R. Parashkov, E. Becker, S. Hartmann, G. Ginev, D. Schneider, H. Krautwald, T. Dobbertin, D. Metzdorf, F. Brunetti, C. Schildknecht, A. Kammoun, M. Brandes, T. Riedl, H. H. Johannes, and W. Kowalsky, Appl. Phys. Lett. **82**(25), 4579 (2003).
[4]N. Stutzmann, R. H. Friend, and H. Sirringhaus, Science **299**(5614), 1881 (2003).
[5]T. Takano, H. Yamauchi, M. Iizuka, M. Nakamura, and K. Kudo, Applied Physics Express **2**(7), 071501 (2009).
[6]M. Uno, Y. Tominari, and J. Takeya, Appl. Phys. Lett. **93**(17), 173301 (2008).
[7]J. Zaumseil and H. Sirringhaus, Chem. Rev. **107**(4), 1296 (2007).
[8]L. P. Ma and Y. Yang, Appl. Phys. Lett. **85**(21), 5084 (2004).
[9]J. Jiang, J. Sun, B. Zhou, A. X. Lu, and Q. Wan, Appl. Phys. Lett. **97**(5), 052104 (2010).
[10]J. Sun, Q. Wan, A. X. Lu, and J. Jiang, Appl. Phys. Lett. **95**(22), 222108 (2009).
[11]J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. Y. He, M. J. Renn, T. P. Lodge, and C. D. Frisbie, Nature Materials **7**(11), 900 (2008).
[12]A. J. Ben-Sasson, E. Avnon, E. Ploshnik, O. Globerman, R. Shenhar, G. L. Frey, and N. Tessler, Appl. Phys. Lett. **95**(21), 3 (2009).
[13]N. Tessler, R. Shenhar, and O. Globerman, U.S. Patent application, 60/756, 997; (2007).
[14]B. Liu, M. A. McCarthy, Y. Yoon, D. Y. Kim, Z. C. Wu, F. So, P. H. Holloway, J. R. Reynolds, J. Guo, and A. G. Rinzler, Adv. Mater. **20**(19), 3605 (2008).
[15]M. A. McCarthy, B. Liu, and A. G. Rinzler, Nano Lett. **10**(9), 3467 (2010).
[16]M. A. McCarthy, B. Liu, R. Jayaraman, S. M. Gilbert, D. Y. Kim, F. So, and A. G. Rinzler, ACS Nano **5**(1), 291 (2011).
[17]K. Aissou, M. Kogelschatz, T. Baron, and P. Gentile, Surf. Sci. **601**(13), 2611 (2007).
[18]M. J. Fasolka and A. M. Mayes, Ann. Rev. Mater. Res. **31**, 323 (2001).
[19]Y. Roichman and N. Tessler, Appl. Phys. Lett. **80**(11), 1948 (2002).
[20]D. J. Pinner, R. H. Friend, and N. Tessler, J. Appl. Phys. **86**(9), 5116 (1999).
[21]Y. Preezant and N. Tessler, J. Appl. Phys. **93**(4), 2059 (2003).
[22]J.-H. Lee, J.-H. Jeong, C.-H. Suh, Y. K. Kim, N. G. Park, and Y. S. Kim, Curr. Appl.Phys. **6**(4), 654 (2006).
[23]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[24]A. N. Tikhonov and A. A. Samarskii, *Equations of Mathematical Physics* (Dover Publications, New York, 1963).
[25]D. L. Scharfetter and H. K. Gummel, IEEE Trans. Electron Devices **16**(1), 64 (1969).
[26]J. Ueda, Y. Namba, K. Sakamoto, T. Miyoshi, and S. Ushio, Electronics and Communications in Japan (Part II: Electronics) **68**(3), 76 (1985).
[27]S. Selberherr, *Analysis and Simulation of Semiconductor Devices* (Springer-Verlag, Vienna, 1984).
[28]B. Pevzner, *Transport and Dielectric Properties of Thin Fullerene (C60) Film* (Massachusetts Institute of Technology, 1995).
[29]M. A. Lampert and P. Mark, *Current Iinjection in Solids* (Academic Press, New York, 1970).
[30]T. B. Singh, N. S. Sariciftci, H. Yang, L. Yang, B. Plochberger, and H. Sitter, Applied Physics Letters **90**(21), 213512 (2007).
[31]G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, and M. Hajlaoui, Adv. Mater. **10**(12), 923 (1998).
[32]E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B. H. Huisman, D. M. de Leeuw, and T. M. Klapwijk, Appl. Phys. Lett. **80**(20), 3838 (2002).
[33]Y. Preezant, Y. Roichman, and N. Tessler, J. Phys. Cond. Matt. **14**, 9913 (2002).
[34]M. Leufgen, U. Bass, T. Muck, T. Borzenko, G. Schmidt, J. Geurts, V. Wagner, and L. W. Molenkamp, Synth. Met. **146**(3), 341 (2004).
[35]A. Hoppe, T. Balster, T. Muck, and V. Wagner, Phys. Status Solidi A-Appl. Mater. Sci. **205**(3), 612 (2008).

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