Temperature Sensitivity of SOI-CMOS Transistors for Use in Uncooled Thermal Sensing

Eran Socher, Salomon Michel Beer, and Yael Nemirovsky, *Fellow, IEEE*

***Abstract*—The temperature coefficient of current (TCC) of CMOS transistors implemented on silicon-on-insulator substrates is theoretically and empirically studied for its potential use in uncooled thermal sensing. Modeling and measurements show TCC values in subthreshold of more than 6%/K, better than state of the art microbolometer temperature coefficient of resistance, and less than −0.4%/K in saturation—comparable with metals. Models and measurements are shown for the TCC dependence upon operating point, temperature and channel length. A simple semi-empirical model for the TCC at subthreshold based on long channel approximation is suggested and shown to agree with measurements for channel length down to 0.35 μm. The model and measurements show a logarithmic tradeoff between subthreshold current and the TCC, which is important in the design of sensors.**

***Index Terms*—CMOS, silicon-on-insulator (SOI), temperature coefficient of current, thermal censors.**

I. Introduction

THE CMOS transistors, used extensively in digital and analog circuit applications find still more uses in sensing applications as sensing elements as well [1]. Driven by both performance and cost, CMOS compatibility of sensors is a major benefit [2]. One of these applications is uncooled thermal sensing. Thermal sensors are sensors that detect radiation indirectly by measuring the temperature change of a thermal mass that absorbs radiation [3]. Thermal sensors achieved a renaissance in the past decade with the assistance of the revolution of micromachining [4]. Micromachining enables the realization of miniature thermally isolated sensor pixels, necessary for uncooled sensitivities approaching that of cooled devices yet with response times short enough for video image rates.

Various sensing elements have been used in thermal sensors, the leading being thermistors [4]–[10], ferroelectric capacitors [11]–[18] and thermocouples [19]–[29]. State of the art sensor arrays make use of microbolometers based upon VO_x thermistors made by post-processing and surface micromachining on top of a CMOS chip containing the readout circuits [8]. However, state-of-the-art thermal sensors are based on materials that are not part of CMOS processing [8], [10], [13]. Current CMOS compatible thermal sensors, based on thermocouples [19]–[29], and microbolometers [6], [30], do not achieve the sensitivity of VO_x microbolometers, which is determined to a large extent by the material absolute temperature coefficient of resistance (TCR) of about 2%/K.

Recently [31], [32], a different approach was proposed based on the use of suspended CMOS transistors in subthreshold. CMOS transistors show high temperature coefficient of current (TCC) values in subthreshold, exceeding state of the art TCR values, thus enabling high performance uncooled thermal sensing in CMOS compatible technology. The use of CMOS transistors offers other advantages, such as using the sensor pixel for multiplexing as well as sensing. The use of CMOS transistors in SOI substrates enables simpler under-etching of devices to release the suspended transistors and to obtain an effective thermal isolation from the silicon bulk, which is necessary for high performance thermal sensing.

This paper deals with the modeling and characterization of the achievable high TCC of standard CMOS transistors implemented in silicon-on-insulator (SOI) substrates, with emphasis on subthreshold. The TCC dependence upon device type, size, operation point and temperature is shown and a simple design model is suggested and verified using measurements. The suggested model, based on long-channel approximations, does not aim to cover the general behavior of the transistor, but rather serve as an effective and practical tool to assess the device TCC and its dependence upon design parameters analytically or semi-empirically.

II. TCC Modeling for Long-Channel CMOS Devices

The drain current temperature dependence of standard CMOS transistors is derived from three main sources: the threshold voltage, the inversion layer charge concentration and the mobility. The threshold voltage depends upon temperature is obtained from the well-established expression [33]

$$V_T = \phi_{\mathrm{MS}} - \frac{qN_{\mathrm{ss}}}{C_{\mathrm{ox}}} + 2\phi_F + \sqrt{\frac{4qN_B\varepsilon_O\varepsilon_S\phi_F}{C_{\mathrm{ox}}^2}} \quad (1)$$

where ϕ_{MS} is the Fermi potential difference between the gate and bulk materials, N_B is the substrate doping, C_{ox} is the gate capacitance, q is the electron charge, ε_0 is the vacuum permittivity, ε_S is the relative permittivity of silicon, and ϕ_F is the Fermi potential of the bulk. The temperature dependence is mainly due to the energy gap temperature dependence, causing the threshold voltage to change about a millivolt per degree. The charge concentration in the inversion layer may change by several percents per degree below the threshold voltage and only

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The authors are with the Department of Electrical Engineering, Technion—Israel Institute of Technology, Haifa 32000, Israel (e-mail: nemirov@ee.technion.ac.il).

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negligibly in saturation or the linear regime [33]. The inversion layer effective mobility depends on temperature according to [33]

$$\mu^* = \mu_0 \left(\frac{T_0}{T}\right)^{\mathrm{b}} \tag{2}$$

where b is typically between 1 and 2 around room temperature, causing the mobility to decrease by about half a percent per degree. The expression for the channel mobility can be further complicated by introducing velocity saturation and mobility degradation [33], [34]. This would mean that the mobility at the reference temperature $\mu_0 = \mu(\mathrm{T}_0)$ depends upon the bias voltages and the threshold voltage and hence upon temperature again. However, that temperature dependence is not significant around room temperature, especially if the normalized derivative $(1/\mu^*)(d\mu^*/dT)$ is considered [33], [34], which is the case below.

Assuming a long channel transistor, the current in the *linear* region of operation is given by [33]

$$I_{\mathrm{DS,linear}} = k\left[(V_{\mathrm{GS}} - V_T)V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2}\right]$$
$$k = \mu^* C_{\mathrm{ox}} \frac{W}{L} \tag{3}$$

where μ^* is the effective channel mobility, C_{ox} is the gate capacitance per unit area and *W* and *L* are the channel width and length, respectively.

When considering the transistor figure of merit for temperature sensing, the equivalent figure to the bolometer TCR is the TCC given by $\mathrm{TCC} = ((1/I_{\mathrm{DS}})(dI_{\mathrm{DS}}/dT))$. In the linear region, this figure yields

$$\mathrm{TCC}_{\mathrm{linear}} = \left(\frac{1}{I_{\mathrm{DS}}}\frac{dI_{\mathrm{DS}}}{dT}\right)_{\mathrm{linear}} = \frac{1}{\mu^*}\frac{d\mu^*}{dT} - \frac{1}{V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}}\frac{dV_T}{dT}. \tag{4}$$

The mobility sensitivity with temperature yields a negative TCC that is compensated by the temperature dependence of the threshold voltage [which is negative in NMOS and positive in PMOS, making the second term of (4) negative in both]. The absolute TCC increases toward the absolute mobility sensitivity as the transistor becomes more conductive with increasing V_{GS} and more linear with decreasing V_{DS}.

In the *saturation* region, the current under the long channel approximation takes the form of [33]

$$I_{\mathrm{DS,sat}} = \frac{k}{2}(V_{\mathrm{GS}} - V_T)^2. \tag{5}$$

The TCC in this region yields

$$\mathrm{TCC}_{\mathrm{sat}} = \left(\frac{1}{I_{\mathrm{DS}}}\frac{dI_{\mathrm{DS}}}{dT}\right)_{\mathrm{sat}} = \frac{1}{\mu^*}\frac{d\mu^*}{dT} - \frac{2}{V_{\mathrm{GS}} - V_T}\frac{dV_T}{dT}. \tag{6}$$

This relative change is a negative few thousandths per degree, which is comparable with most of the metals used in bolometers, again due to the negative mobility sensitivity, compensated by the negative V_T temperature coefficient in an NMOS device. In PMOS devices the threshold voltage has a positive temperature coefficient but $V_{\mathrm{GS}} - V_T < 0$ so the sign of the TCC remains. The TCC may reach zero (zero temperature coefficient point or ZTC) for small enough V_{GS}, given approximately by [using (6)]

$$V_{\mathrm{GS,ZTC}} = V_T + \frac{2\frac{dV_T}{dT}}{\frac{1}{\mu^*}\frac{\mathrm{d}\mu^*}{dT}}. \tag{7}$$

This critical V_{GS} is typically hundreds of millivolts above V_T. The exact value is influenced by subthreshold behavior around V_T, making the use of a more elaborate model necessary [33].

In the *subthreshold* region in NMOS, the current has the typical exponential form of [33]

$$I_{\mathrm{DS,sub}} = \mathrm{k}\left(\frac{k_BT}{q}\right)^2 (n-1)e^{\frac{q}{\mathrm{nk_B}T}(V_{\mathrm{GS}}-V_T)}\left(1 - e^{-\frac{qV_{\mathrm{DS}}}{k_BT}}\right) \tag{8}$$

where $n = 1 + (C_S + C_{\mathrm{it}})/C_{\mathrm{ox}}$ and C_S, C_{it} and C_{ox} are the semiconductor, fast surface states and oxide capacitance, respectively. This parameter is easily characterized by the transistor swing. Equation (8) holds for PMOS as well if absolute values of voltages and the current are taken. Due to the exponential dependence upon the threshold voltage (assuming $V_{\mathrm{DS}} \gg k_B$T/q), the TCC becomes

$$\mathrm{TCC}_{\mathrm{sub}} = \left(\frac{1}{I_{\mathrm{DS}}}\frac{dI_{\mathrm{DS}}}{dT}\right)_{\mathrm{sub}} = \frac{1}{\mu^*}\frac{d\mu^*}{dT} + \frac{2}{T} - \frac{q}{nk_BT}\left[\frac{dV_T}{dT} + \frac{V_{\mathrm{GS}} - V_T}{T}\right]. \tag{9}$$

In NMOS devices, the TCC is positive mainly due to the V_T negative temperature dependence and compensated by the mobility temperature sensitivity. Equation (9) applies for NMOS devices, but can be used for PMOS devices if voltages are taken in absolute values. The distance of V_{GS} from V_T further increases the TCC as the transistor goes deeper into weaker inversion, yielding TCCs of 6% per degree and more, which is better than state of the art bolometer materials, such as vanadium oxide [4]. Equation (9) can be rewritten as a function of the transistor current instead of the gate bias

$$\mathrm{TCC}_{\mathrm{sub}} = \left(\frac{1}{I_{\mathrm{DS}}}\frac{dI_{\mathrm{DS}}}{dT}\right)_{\mathrm{sub}} = \frac{1}{\mu^*}\frac{d\mu^*}{dT} + \frac{2}{T} - \frac{q}{nk_BT}\frac{dV_T}{dT} - \frac{1}{T}\ln\left[\frac{I_{\mathrm{DS}}L}{W\mu^* C_{\mathrm{ox}}(n-1)}\left(\frac{q}{k_BT}\right)^2\right]. \tag{10}$$

The mobility temperature coefficient would be simply −b/T according to (2), the threshold temperature slope is fairly constant with temperature and the natural log makes temperature dependencies other than that of the current negligible. The result is a semi-empirical relation of the subthreshold TCC

$$\mathrm{TCC}_{\mathrm{sub}} = \left(\frac{1}{I_{\mathrm{DS}}}\frac{dI_{\mathrm{DS}}}{dT}\right)_{\mathrm{sub}} = \frac{A}{T} - \frac{B}{T}\ln\left[\frac{I_{\mathrm{DS}}L}{I_0W}\right] \tag{11}$$

TABLE I
SUMMARY OF TESTED TMOS DEVICES TYPE AND SIZE

Transistor type	Symbolic name	Width [μm]	Length [μm]
NMOS	N1	10	0.35
	N2	10	0.5
	N3	10	0.8
	N4	10	2
	N5	10	10
PMOS	P1	10	0.35
	P2	10	0.5
	P3	10	0.8
	P4	10	2
	P5	10	10

where *A, B,* and I_0 are technology based coefficients. The theoretical values of *A, B,* and I_0 according to the long channel model of (10) are

$$\mathrm{A} = 2 - b - \frac{q}{nk_B}\frac{dV_T}{dT} B = 1 I_0 = \mu^* C_{\mathrm{ox}}(n-1)\left(\frac{k_B T}{\mathrm{q}}\right)^2. \quad (12)$$

Long-channel SOI devices deviate standard CMOS devices as the thickness of the SOI device layer (serving as the transistor bulk) decreases [35]–[38]. With decreasing thickness, the nature of the transistor shifts from partially depleted to fully depleted, making the semiconductor capacitance contribution to n smaller, thus lowering its value closer to the ideal value of 1 and making the subthreshold slope steeper. The thickness of the SOI device layer would also affect the value of the threshold voltage and weaken its temperature dependence, but not the validity of the above analysis. According to (11) and (12), reducing n and lowering the temperature dependence of the threshold voltage may increase or decrease the resulting TCC values, depending on the exact values.

III. Description of Devices Under Study

In order to compare the TCC modeling with measured results, devices were fabricated. The process in which the transistors were fabricated was the TS35 0.35-μm analog process of Tower Semiconductors [39]. This process is optimized for analog and sensor applications by enabling low noise transistors and other analog options such as linear capacitors and high resistance resistors. The process was carried out according to a specific design on special SOI substrates of 575-μm-thick silicon handle wafer with a 2-μm-thick buried oxide layer and a 2-μm-thick silicon device layer compatible with a TS35 epilayer process. The substrates were supplied by CANON and fabricated using their ELTRAN process [40] that involves oxidized wafer bonding and water-jet separation using a predefined porous silicon layer.

Since the device layer thickness is larger than the depth of the source/drain and even the well implantations of the CMOS process and the buried oxide is much thicker than the gate oxide, SOI effects on the model of the transistors should not be significant. Indeed, characterization showed the transistors performance is within the standard CMOS specification for this process.

Several NMOS and PMOS devices were selected for the temperature dependent characterization. The devices size and notation are summarized in Table I. All devices were chosen with a channel width of 10 μm so that current would be high enough

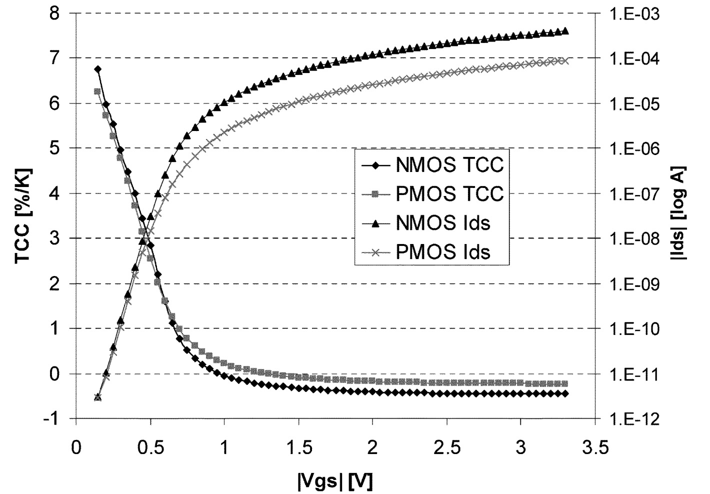

Fig. 1. Measured NMOS and PMOS transistor TCC and $|I_{\mathrm{DS}}|$ versus $|V_{\mathrm{GS}}|$ for transistor size of 10 μm/10 μm and $V_{\mathrm{DS}} = 3$ V at T = 25 °C.

for accurate measurement and in order to eliminate the transistor narrow channel effects on performance. Transistors differ in channel length in order to estimate the TCC dependence on this parameter that enables an increase in current signal and a reduction in size. The range of channel lengths enables testing of both short channel and long channel devices.

All devices currents were measured in the temperature range of 20 °C–70 °C with 5 °C steps. At each temperature gate and drain voltage sweeps were conducted in the range of 0–3.3 V (for gate bias) and 0–3.6 V (for drain bias). The TCC was evaluated from the measurements using the derivative of the natural logarithm of the interpolation function around each temperature point.

IV. Gate Bias Dependence of the TCC

One of the main dependencies of the TCC is the dependence upon the gate voltage. For high enough drain bias, it is the gate bias that determines whether the transistor is in subthreshold, saturation or linear state. From the analytical study we expect significant and positive TCC at subthreshold and negative and relatively small TCC at saturation and linear states.

Fig. 1 shows the measured gate bias dependence of the TCC and the drain current for both NMOS and PMOS transistors. The drain was biased with 3 V to avoid the linear state, the devices chosen are with $L = 10$ μm to avoid short channel effects and temperature is set at 25 °C. Fig. 1 shows TCCs approaching 7%/K for both NMOS and PMOS devices in deep subthreshold. The apparent limitation is the very small currents associated with these high TCCs. More reasonable drain currents of 10 nA yield a more moderate, but still attractive, TCC of about 3%/K. The NMOS device achieves of course larger currents across the bias range, but also exhibits larger TCCs both at subthreshold and saturation.

The smaller absolute TCC of the PMOS device in saturation suggests a less significant channel mobility temperature coefficient (with b of about 1) of holes compared to electrons in the NMOS channel (with b of about 1.5). While the subthreshold current slope suggests an n of 1.44 in NMOS and 1.52 in PMOS, fitting the TCC behavior with V_{GS} against (9) yields an effective

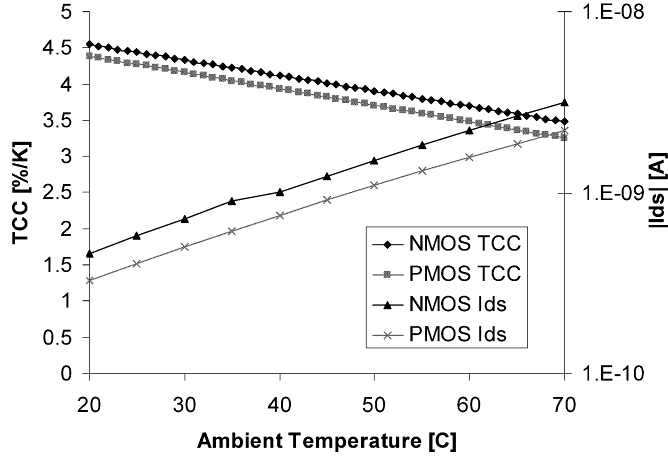

Fig. 2. Measured NMOS and PMOS transistor TCC and $|I_{\rm DS}|$ versus ambient temperature for transistor size of 10 /10 μm, $V_{\rm GS} = 0.35$ V and $V_{\rm DS} = 3$ V.

of 1.2 for NMOS and 1.23 for PMOS devices. The PMOS device shows a higher n than the NMOS mainly due to its higher bulk doping. The lower n derived from the fit to (9) could be explained by the simplified model that was used in its derivation. Still, it can be used semi-empirically to describe the TCC behavior at subthreshold.

V. Temperature Dependence of Subthreshold TCC

According to (9), the temperature dependence of the TCC for a specific operation point can be derived as

$$\frac{d(\mathrm{TCC_{sub}})}{dT} = -\frac{2-b}{T^2} + \frac{2q}{nk_BT^2} \times \left[\frac{dV_T}{dT} + \frac{V_{\rm GS}-V_T}{T}\right] - \frac{\mathrm{q}}{nk_BT}\frac{d^2V_T}{dT^2}. \quad (13)$$

Fig. 2 exhibits the temperature dependence of the TCC for the devices investigated in Fig. 1. Normally, bolometers and other temperature sensitive devices used as IR thermal sensors are operated in a temperature stabilized environment, so the temperature sensitivity of the TCR (or the TCC) should not be important. However, with the desire to reduce cost, more and more applications operate with temperature compensation rather than stabilization. Temperature sensitivity of the TCC is then highly important. Fig. 2 shows that the TCC temperature sensitivity in subthreshold is about $0.02\%/\mathrm{K}^2$ in both PMOS and NMOS devices, which is corroborated by (13) as well for these devices. This moderate and known change in TCC allows for easy temperature gain compensation. However, the transistor current shows significant increase with temperature, as expected due to the high TCC, thus posing a difficult problem for readout circuits that are meant to compensate for temperature changes rather than rely on temperature stabilization. A possible solution in this case could be active biasing of the transistor.

VI. Channel Length and Drain Bias Dependence

Shrinkage of the CMOS transistor offers many advantages in both digital and analog applications, but also to their use as sensors. Fabrication of a smaller transistor with similar performance offers the possibility of smaller sensor pixels that

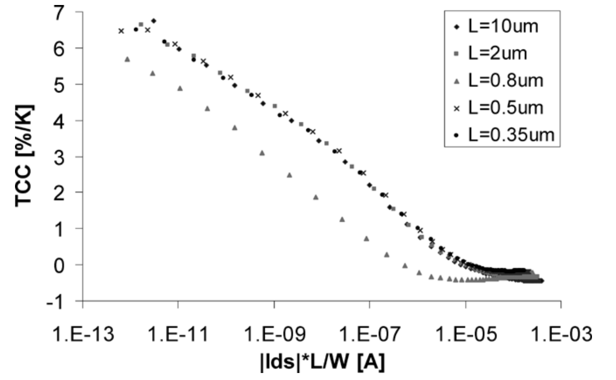

Fig. 3. Measured NMOS transistor TCC versus $|I_{\rm DS}| * L/W$ for transistor channel width of 10 μm and varying length with $V_{\rm DS} = 3$ V and $T = 25$ °C.

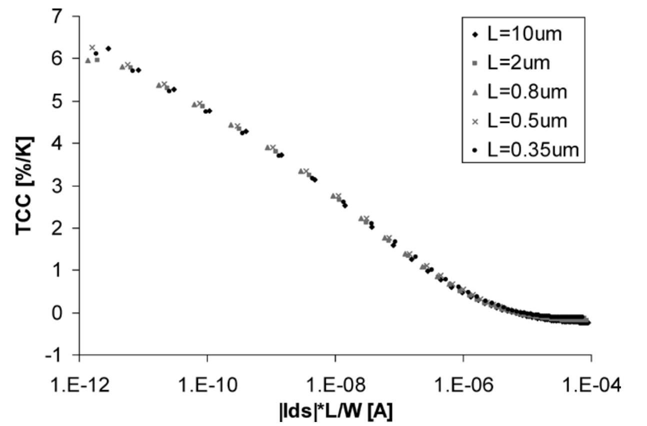

Fig. 4. Measured PMOS transistor TCC versus $|I_{\rm DS}| * L/W$ for transistor channel width of 10 μm and varying length with $V_{\rm DS} = 3$ V and $T = 25$ °C.

achieve better spatial resolution and enable shorter response time due to the smaller thermal mass. However, smaller devices, especially with shorter channel length, need more sophisticated modeling due to short channel effects. Among the short channel effects relevant to channel lengths down to 0.35 μm we can name channel length modulation, drain induced barrier lowering and velocity saturation [33]. It is therefore necessary to verify the validity of the simple TCC model in the case of shorter devices, especially with increasing drain bias.

Figs. 3 and 4 show the channel length dependence of the TCC versus $I_{\rm DS}$ current relation. As was shown in Fig. 1, high and positive TCC is achieved for very low currents while the transistor is in deep subthreshold. As the current is increased by applying larger $V_{\rm GS}$, the TCC decreases gradually and changes its sign while the transistor steps out of subthreshold and enters saturation. Figs. 3 and 4 present the relation between the TCC and the transistor current for NMOS and PMOS transistors, respectively, at room temperature and $V_{\rm DS} = 3$ V. The current is normalized by multiplying by *L/W* for each device so that short channel effects would be more apparent without showing the obvious current scaling. The different curves shown represent transistors with varying channel length L between 0.35 and 10 μm. Sensors based on CMOS transistors used as temperature sensors would benefit from current increase in the transistor if the TCC remains the same since the transistor current change would be larger for a given temperature change. Therefore, since Figs. 3

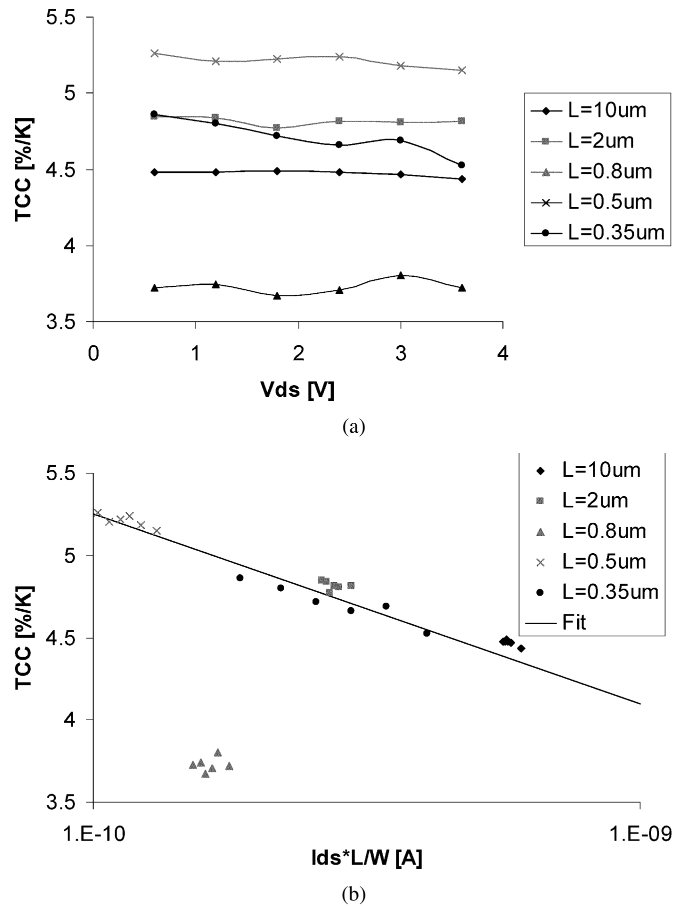

Fig. 5. (a) Measured NMOS transistor TCC versus $V_{\rm DS}$ for transistor channel width of 10 μm and varying length with $V_{\rm GS} = 0.35$ V and $T = 25$ °C. (b) Measured NMOS transistor TCC versus $I_{\rm DS} * L/W$ for transistor channel width of 10 μm and varying length with $V_{\rm GS} = 0.35$ V and $T = 25$ °C.

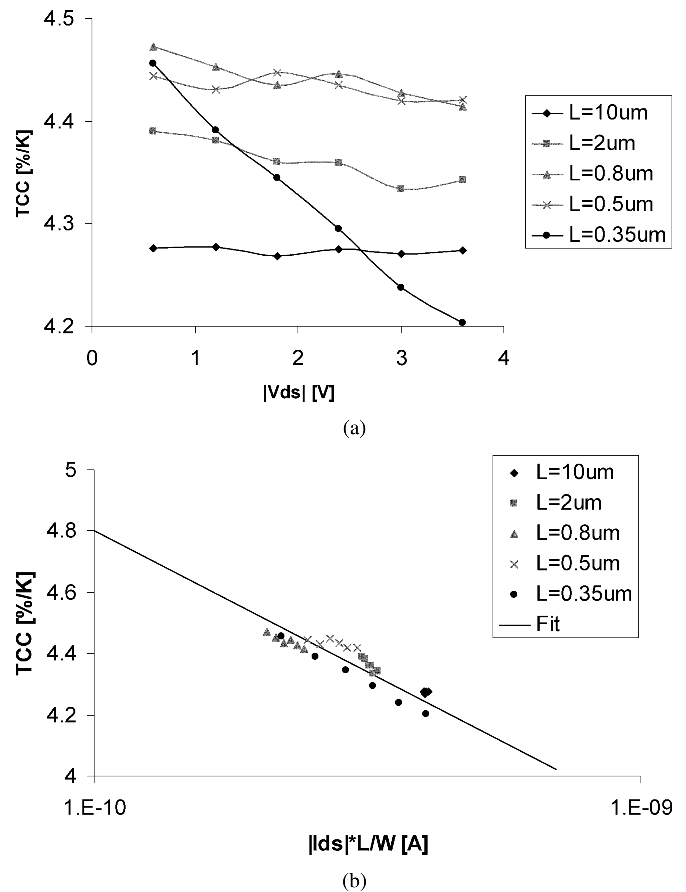

Fig. 6. (a) Measured PMOS transistor TCC versus $|V_{\rm DS}|$ for transistor channel width of 10 μm and varying length with $V_{\rm GS} = -0.35$ V and $T = 25$ °C. (b) Measured PMOS transistor TCC versus $|I_{\rm DS}| * L/W$ for transistor channel width of 10 μm and varying length with $V_{\rm GS} = -0.35$ V and $T = 25$ °C.

and 4 show that transistor TCC is found not to be affected by the channel length L (for a given normalized current), current can easily be increased by reducing it, thus improving performance.

Exceptions to the general trend in subthreshold include the behavior in $V_{\rm GS} < 0.25$ V, in which measurement errors are more significant, and the NMOS with $L = 0.8$ μm, which has much less current than expected and its performance is outside the process corners. Measurements thus show that neglecting short channel effect does not significantly affect the estimation of the TCC at subthreshold using (10) or (11). It should be noted that plotting the TCC as a function of $V_{\rm GS}$ would show differences between transistors, but these are mainly due to the process variations in V_T. Plotting the TCC against the current eliminates most of the effect of the threshold voltage process variations and the behavior of (10) holds. A better fit to (10) would be achieved using (11) with *B* parameters of 1.1 for the NMOS devices and 1.2 for the PMOS devices, instead of the default value of 1. In saturation, however, the TCC approaches zero as the channel length is reduced, a behavior which requires short channel effect modeling.

Figs. 5 and 6 show the subthreshold TCC dependence upon the drain bias for NMOS and PMOS transistor with different channel length. In Fig. 5(a) the dependence is shown for the NMOS devices and it can be seen that for all channel lengths, except for $L = 0.35$ μm, the TCC does not change much over the drain bias range of 0.6–3.6 V (about -0.01%/kV up to -0.03%/kV for the 0.5 μm device). This corresponds to a relatively small effective λ (channel length modulation) parameter calculated for these devices from measurements, which achieves an L dependence of $0.056/L^{0.43}V^{-1}$, where L is in micrometers. The 0.35-μm-channel device differs in that manner. Both its effective λ parameter (0.39 V^{-1}) and the TCC slope with the bias (-0.1%/kV) are much more significant, due to short channel effects. Again, we note the 0.8 μm-channel device is outside the process corner. Fig. 5(b) shows the TCC dependence against the transistor normalized current, which is also affected by λ. Since the major effect of the drain voltage on the subthreshold current is through the change in the threshold voltage drain-induced barrier lowering (DIBL) [33], relating the TCC change again to the change in $\ln(I_{\rm DS})$ is logical, according to (10) or (11). Indeed, Fig. 5(b) shows a linear relation between the TCC and $\ln(I_{\rm DS})$ with a fitted *B* parameter of about 1.1. Even the device with a channel length of 0.35 μm, which has more significant short channel effects, follows the predicted trend.

In Fig. 6(a) the dependence is shown for the PMOS devices and it can be seen that again for all channel lengths, except for $L = 0.35$ μm, the TCC does not change much over the

drain bias range of 0.6–3.6 V (about -0.01%/kV). This corresponds again to a relatively small effective λ that can be expressed as $0.043/L^{0.86}V^{-1}$. The 0.35 μm—channel device is different again. Its λ parameter (0.28 V^{-1}) and its TCC slope with the bias (-0.085%/kV) are much more significant, due to short channel effects. However, as can be seen in Fig. 6(b), the TCC dependence against the transistor normalized current follows a similar trend to that of NMOS devices. Using the empirical fit of (11) yields a B parameter of about 1.2. Larger deviations are seen from the simple fit due to the measurement errors related to the smaller currents in PMOS devices compared with NMOS devices.

VII. Summary

In this paper, the TCC of SOI-CMOS transistors was modeled and characterized in a wide range of operation points, temperatures and device sizes for use in the design of uncooled thermal sensors. Modeling and characterization showed achievable TCC of more than 6%/K in subthreshold and less than -0.4%/K in saturation. The TCC in subthreshold is better than the comparable TCR in state of the art microbolometer technology. A semi-empirical model, relating the TCC in subthreshold to the drain current based on long channel models, proved to be useful for long as well as short channel devices in a variety of operation points and temperatures. The model also proved useful in eliminating the dependence upon threshold voltage tolerance in the estimation of the TCC. Modeling and measurement show the logarithmic tradeoff between transistor current and the TCC. Temperature has a small effect on the subthreshold TCC although a significant effect on the current itself exists due to the high TCC. Characterization shows small dependence of transistor normalized current and TCC upon channel length down to $L = 0.5$ μm and significant current change in 0.35-μm devices. However, all devices followed the TCC trend with transistor current predicted by the simple semi-empirical design model based on long channel approximation. Due to the relatively thick SOI layer, transistor performance complied with standard CMOS models. Expected results in thinner SOI device layers should comply with the semi-empirical model for the TCC, while the smaller n values (corresponding to a higher subthreshold slope) may increase the TCC values in subthreshold. A way of explaining the validity of the analysis based on a simplified transistor model may be that the TCC is normalized current sensitivity, and as such, a factor that have significant effect of the current have similar effect on the current derivative with temperature. As a result, short channel and other advanced CMOS effects have fairly insignificant effect on the TCC. On the other hand, complicating the equation even with "simple" effects, such as mobility degradation and velocity saturation, inhibits the formulation of an expression for the TCC that would be useful as a design tool. Introducing complications into the model to achieve better fits without losing practicality may still be a challenge. The results of the study suggest that thermal sensors based on CMOS transistors may achieve better sensitivity than state of the art microbolometers due to the higher TCC while implemented in standard CMOS technology.

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Eran Socher was born in Tel Aviv, Israel, on December 12, 1975. He received the B.Sc. degree in electrical engineering, the B.A. degree in physics (both *summa cum laude*), and the M.Sc. and Ph.D. degrees in electrical engineering, from the Technion—Israel Institute of Technology, Haifa, Israel.

He is currently with the IDF Research Unit and lecturing at the Technion and Bar-Ilan University. His research focuses on analysis, optimal design, fabrication and characterization of micromachined integrated electro-thermal devices, especially for uncooled IR sensing applications. Other fields of interest are micromachined inertial sensors, analog interface circuits for microsystems, RF-MEMS devices and fundamental noise phenomena in microsystems.

Salomon Michel Beer was born in Montevideo, Uruguay, in April, 1982. He received the B.A. degree in physics and the B.Sc. degree in electrical engineering from Technion—Israel Institute of Technology, Haifa, Israel, in 2004, where he is currently pursuing the M.Sc. degree.

From 2000 to 2004, he was a Member of the Technion Excellence Program. He served as a Teaching Assistant for classes in signal processing and digital circuits. He is currently with Freescale Semiconductor, Israel.

Yael Nemirovsky (F'00) received the D.Sc. degree from Technion—Israel Institute of Technology, Haifa, Israel, in 1971.

She is a Member of the Faculty of Electrical Engineering, Technion. She is a Pioneer of micro-electro-mechanical systems (MEMS) research in Israel and in the last decade her research has focused on micro-opto-electro-mechanical (MOEMS) systems. She has published approximately 170 papers in refereed journals, copresented over 200 talks in conferences and filed for several patents.

Dr. Nemirovsky is a Fellow of the Institute of Electrical Engineers, U.K. She is the recipient of the "The Award for the Security of Israel" and Technion Awards for "Best Teacher" and "Novel Applied Research." She also received the Kidron Foundation Award for "Innovative Applied Research" and the USA R&D 100 2001 Award recognizing the top 100 new inventions and products of the year.