Current skimming-based CMOS readout architectures for Quantum Well Infrared Photodetectors

Calist Friedman[1], Arie Arbel and Ran Ginosar[2]
VLSI Systems Research Center, Electrical Engineering Department
Technion—Israel Institute of Technology
Haifa 32000, Israel
Phone: +972-53-252588, Fax: +972-4-8323041
Email: calist@tx.technion.ac.il

Cost-effective high-performance IR imaging cameras based on Quantum Well Infrared Photodetectors (QWIP) need CMOS readout structures which allow effective operation at temperatures compatible with inexpensive long-life coolers. At such high temperatures (around 72^0 K), the QWIP suffers from large background and dark currents (Fig. 1), which have a tendency to saturate the integrating capacitor in the readout cell.

The present research focuses on evaluating per-pixel current suppression (skimming) concepts, in order to make possible the use of small integration capacitors and avoid their saturation, thereby increasing the dynamic range (Fig. 2) and signal-to-noise ratio of the detector-readout assembly. Such circuits enable per-pixel Adaptive Sensitivity™ operation to further enhance the dynamic range.

The approach investigated in this paper is based on externally controlled partial current skimming (Fig. 3). This scheme consists of a conventional Direct Injection (DI) structure with an additional skimming transistor (M_2) incorporated in each pixel. The input transistor (M_1) ensures high injection efficiency and isolates the detector from the integrating node (A). Both skimming and input transistors are operating in subthreshold. An external voltage (*adjust*) determines the amount of drain current flowing through M_3 and subtracted from the total input current. By adjusting the skimming current to a value close to the sum of background and dark currents, the resulting signal can be reduced close to the interesting ac component (Fig. 2). This technique has the advantage of simplicity and it can be easily incorporated in a small area pixel (Fig. 5). Because the integration current is reduced significantly, C_{int} can be decreased without saturating it.

In the framework of this research, two readout techniques were analyzed and compared: a voltage-readout structure employing a source-follower output stage for driving a per-column sample-and-hold block (Fig. 3) and a current-readout configuration with an output selection transistor interfacing with a per-column integrator stage (Fig. 4). The following points have been observed:

1. Design complexity: For the current-readout approach, the reset operation is "built-in" the readout process thus no reset switch is necessary; also, the output stage comprises only a single transistor while the voltage readout implies an additional transistor. These two observations translate into about 10% lower pixel area for the current-readout structure.

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[1] Currently with Chartered Semiconductor Manufacturing Ltd. Israel
[2] On Sabbatical leave with Intel Corporation, Hillsboro, OR, USA

2. Power consumption: When activated, the source follower stage consumes more power than the simple select switch at the output of the current mode pixel.
3. Noise performance: Simulations and measurements show that the total output noise of the current-readout cell (Fig. 9) is lower than that of the voltage-readout scheme. This difference results from the follower stage M_3 (Fig. 3), which contributes a substantial part of the total output referred noise of the voltage-readout scheme. Furthermore, the voltage offset introduced by the source follower stage of the voltage-readout is absent in the current-readout scheme.

Thus, it can be concluded that the current-readout technique is preferred over the voltage-readout.

During integration, the drain-source voltage of M_2 (Fig. 3 and 4) varies together with the voltage on C_{int}. This variation of V_{DS} causes an increase of I_D in time (short-channel effect), leading to nonlinear behavior. A self-cascoded skimming current-source transistor is employed in order to improve the linearity of per-pixel current skimming (Fig. 8). The gate of the transistor is split into two parts, as shown in Fig. 6. This configuration increases the small-signal output resistance of the simple current sink ($r_{out,simple} = r_{ds2}$) by approximately the common-gate voltage gain of M_{2a}:

$$r_{out,self\text{-}cascode} = g_{m2a}\, r_{ds2a}\, r_{ds2b}$$

where g_{m2a} is the channel transconductance of the upper transistor and $r_{ds2a,2b}$ the small-signal channel resistance of the transistors.

Subsequent to comprehensive simulations, the design was implemented in a prototype integrated circuit (Fig. 11), fabricated through MOSIS in Orbit 2μ CMOS technology. An on-chip controller was incorporated for a complete system-on-a-chip solution. Measurements of this test chip proved the validity of the new readout schemes and demonstrated correct functionality of the detector-readout architecture at higher temperatures than originally planned (namely at higher dark current rates). Fig. 7 presents the voltage-modulated output of an array of 4×4 current-readout pixels operating at $T_{FPA}=84^0\,K$, seeing a uniform scene of $T_A=300^0\,K$.

Black body measurements revealed a good responsivity of the assembly at temperatures as high as $84^0\,K$ (Fig. 10). The responsivity, defined as the ratio of the photosignal (output voltage) to the radiation power incident upon the detector, was measured at 0.81 V/nW.

Generally, the total input referred noise current of the readout assembly is made up of four main components: background optically generated shot noise, detector total noise, input stage noise, and signal processing stage noise. The goal of the current readout structure was to make the latter three noise components less than the background shot noise, facilitating background-limited performance of the QWIP FPA. But at QWIP temperatures higher than $68^0\,K$ the detector total noise (especially the dark current shot noise) is greater than the inevitable background shot noise, determining the BLIP condition to be practically unrealizable. However, the noise introduced by the readout pixel was found to be an order of magnitude lower than the background shot noise, thus fulfilling the main requirement of a readout stage.

In conclusion, the design was demonstrated in silicon to enhance the dynamic range of real QWIP-based FPAs, operating at temperatures approaching $84^0\,K$.
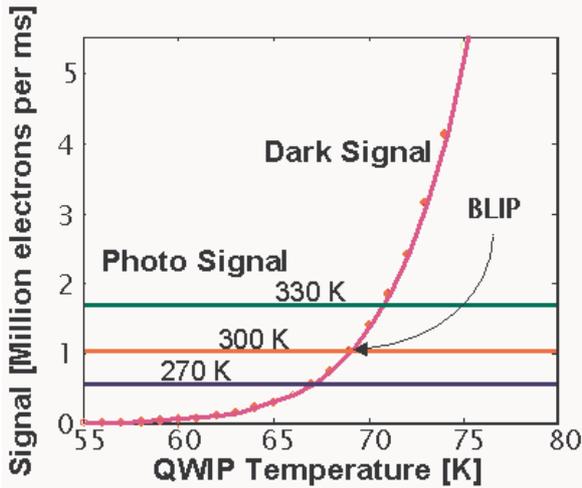
Fig. 1: Photo and dark current signals as a function of temperature for a $\lambda_p = 8.8\ \mu m$ QWIP with an area of $28\times28\ \mu m^2$.
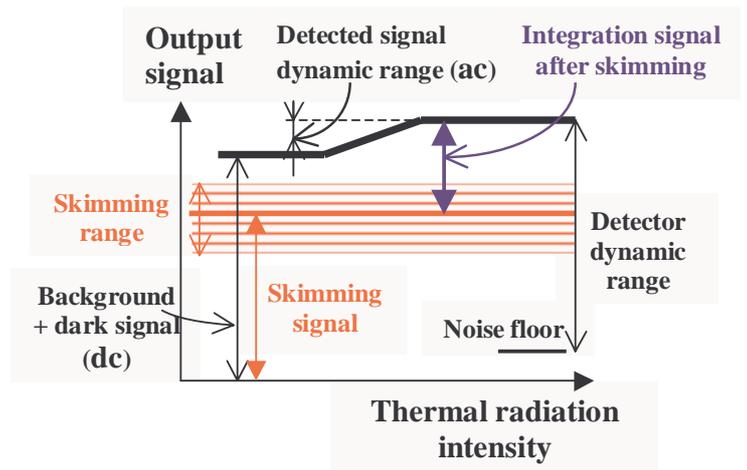

Fig. 2: Externally adjusted skimming concept: a large part of the full dynamic range of the readout circuit is reserved for the important ac signal (at certain temperatures, less than 10% of the total signal)
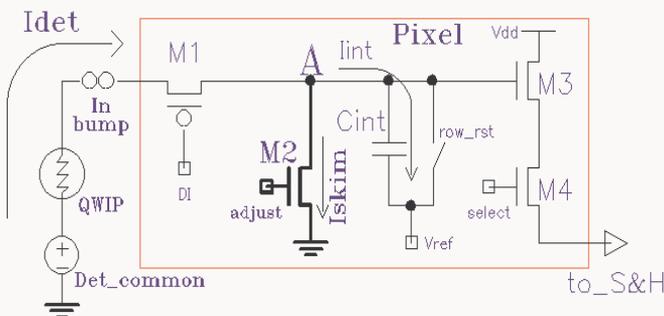

Fig. 3: Voltage readout architecture: A direct injection input transistor, a skimming transistor with external gate-control, per-pixel integration capacitor, and a source-follower output stage with a row-select transistor (the per-column current-source transistor is not shown).
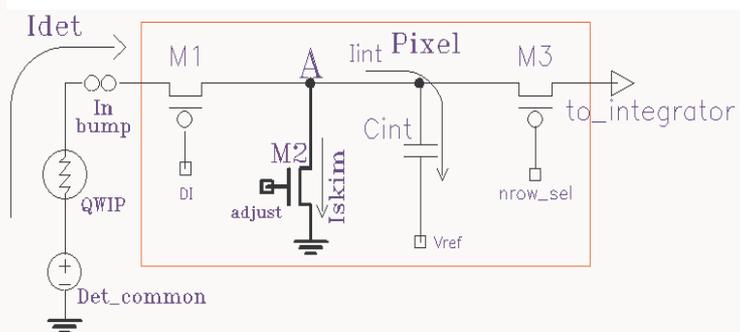

Fig. 4: Current readout architecture: The front-end is similar to the voltage readout scheme; the output current flows through a row-select transistor. The reset of C_{int} is part of the readout operation.
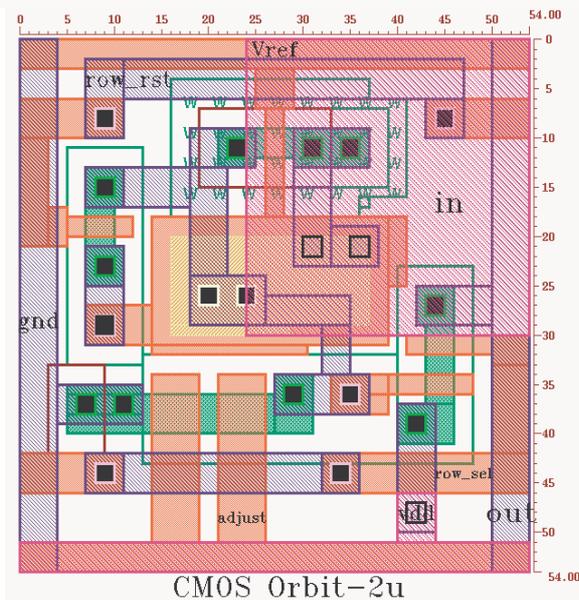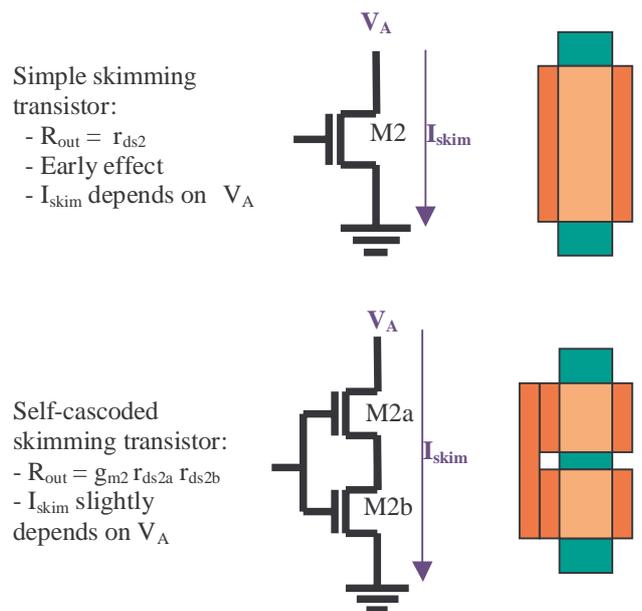

Fig. 5: Layout of a self-cascoded skimming, voltage-readout pixel

Simple skimming transistor:
- $R_{out} = r_{ds2}$
- Early effect
- I_{skim} depends on V_A

Self-cascoded skimming transistor:
- $R_{out} = g_{m2}\, r_{ds2a}\, r_{ds2b}$
- I_{skim} slightly depends on V_A
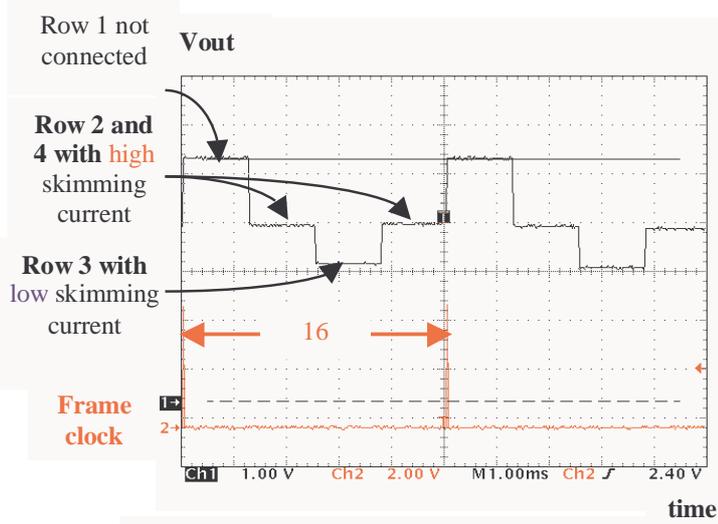
Fig. 6: Simple versus self-cascoded skimming transistors

Row 1 not connected

Vout

Row 2 and 4 with high **skimming current**

Row 3 with low **skimming current**

16

Frame clock

Ch1   1.00 V   Ch2   2.00 V   M1.00ms   Ch2 ∫   2.40 V

time

Fig. 7: Current readout array's serial output, with four identical pixels in a row and seeing the same background (Idc=10µA)

Tek Run: 50.0kS/s   Hi Res

Vcap

Simple skimming transistor

Self-cascoded skimming transistor

Ch2   500mV   M1.00ms   Ch2 ∫   1.43 V
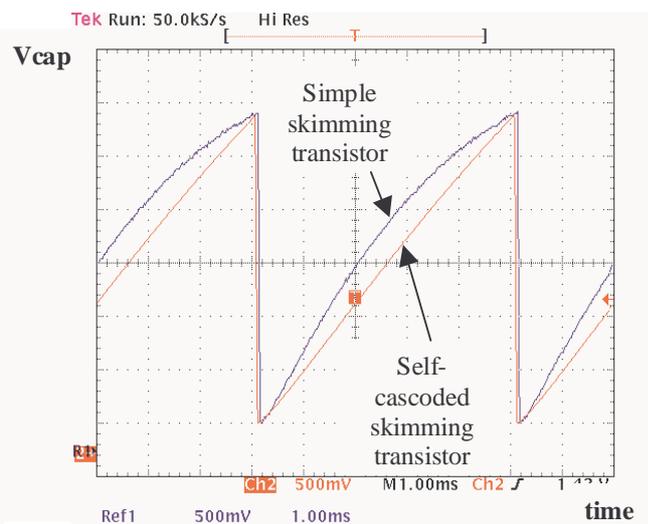Ref1   500mV   1.00ms

time

Fig. 8: Improved linearity of integration in the case of self-cascoded skimming transistor is demonstrated by measuring the voltage on the capacitor **between two consecutive resets**
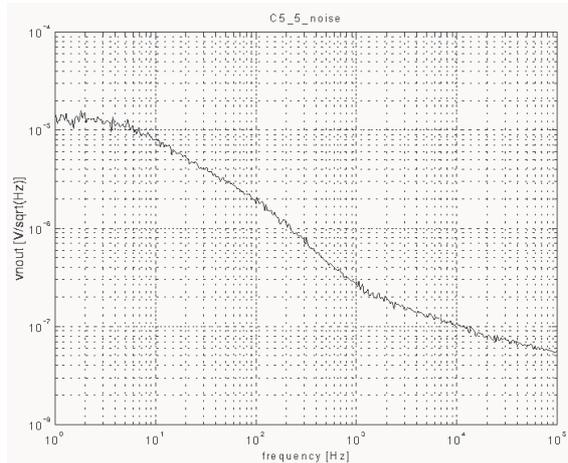
C5_5_noise

vnout [V/sqrt(Hz)]

frequency [Hz]

Fig. 9: Measured total output noise of the current-readout circuit

Responsivity of the sensor-readout assembly

Vout[mV]

ΔV_{out}

ΔP
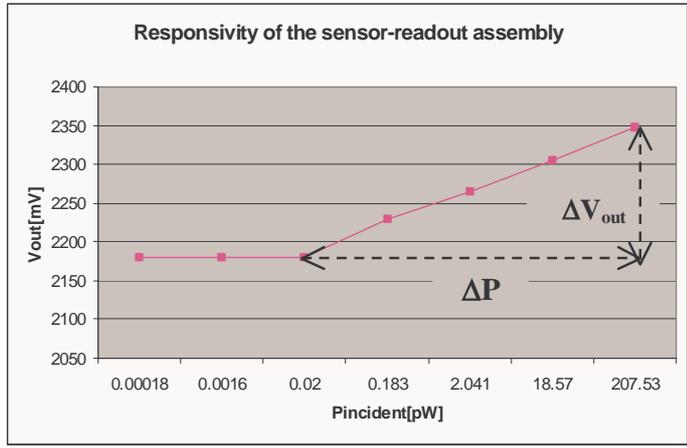
0.00018 0.0016 0.02 0.183 2.041 18.57 207.53
Pincident[pW]

Fig. 10: Output voltage of the **QWIP-readout cell assembly as a function of radiation power incident upon a QWIP at 84⁰K, with 200×200 µm² active area, positioned at 7cm from a black-body of 1000⁰K**

array of 4x4 current readout pixels

test pixels
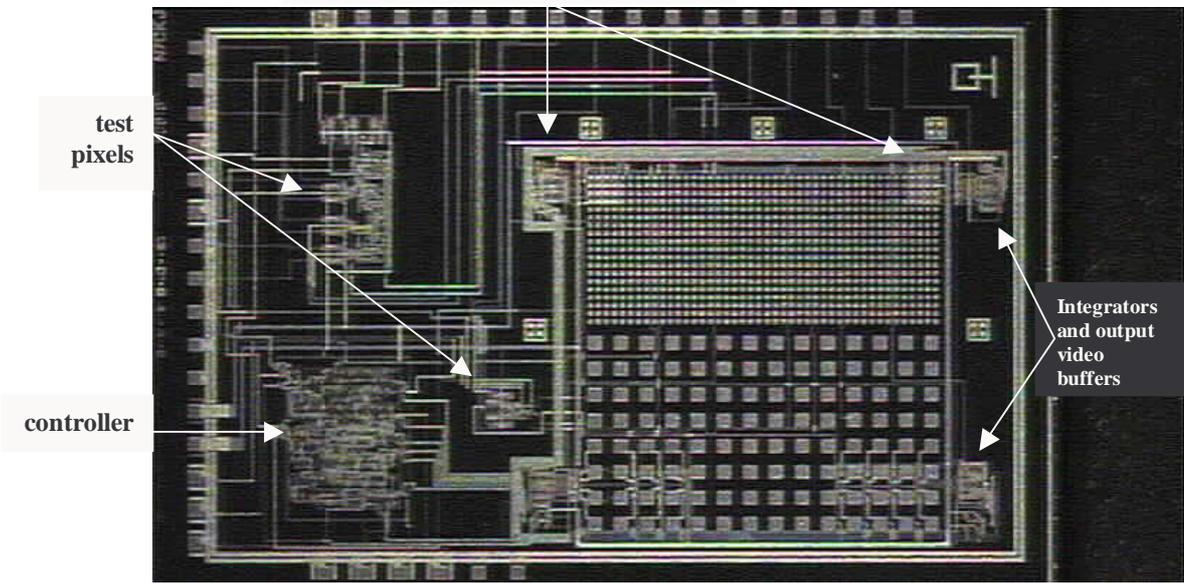
controller

Integrators and output video buffers

Fig. 11: Micro-Photograph of the prototype integrated circuit