Rad-Hard 2.5 Gbps SpaceFibre Interface Device

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Abstract

Seven partner institutions and companies have been cooperating within the scope of the FP7 Collaborative Project VHiSSI to develop a very high speed serial interface device. The device will include two SpaceFibre serial links capable of data rates up to 2.5 Gbps (3.125 Gbps after 8b/10b encoding). Complete SpaceFibre networking stack is implemented in the device. It also provides a variety of other interfaces including SpaceWire, parallel buses, LVTTL and LVDS signaling. Operating modes include SpaceFibre and SpaceWire bridges and routers, interfaces to instruments, to processors and to mass memory. The device is implemented on IHP 130nm CMOS technology, using RadSafe™ rad-hard-by-design libraries and custom analog circuits. A test chip has recently been fabricated and tested to validate the technology and circuits for the SERDES device.

1. SpaceFibre SERDES Project Goals

The Collaborative Project VHiSSI goals include:

- Provide Europe with an ITAR-free technology and devices for high speed serial interconnect on board spacecraft.
- Provide a SERDES for SpaceFibre [1] links, a critical component for utilizing such links.
- Enable a rich variety of options and alternatives for interfacing high performance space bourne digital devices and systems with high speed serial links enabling effective board-to-board and system-to-system interconnects within the spacecraft.
- Develop European technology for advanced rad-hard devices and systems through collaboration of multiple, mostly small, entities.

2. Multi-partner Project

The VHiSSI FP7-funded Collaborative Project combines the following seven partners into an effective and powerful consortium. The space technology Centre at the University of Dundee has initiated and developed SpaceWire and is presently extending that work to developing SpaceFibre, a more advanced networking technology for spacecraft use. Star-Dundee is developing SpaceWire and SpaceFibre systems and digital logic, implementing, investigating and demonstrating the technology developed at the University. Ramon Chips of Israel has developed RadSafe™, a radiation hardening by design technology that has already produced several rad-hard chips for space. ACE-IC, also of Israel, has developed high speed analog circuits such as SERDES and the present project enables them to apply their technology to space applications. Synergie CAD Instruments of Italy is specializing in the testing of high speed circuits such as SERDES. IHP investigates how this technology could be used on their research fabrication facilities. And EADS Astrium, a principal space contractor that develops and manufactures satellites and spacecraft, represents the users' point of view by formulating the requirements, by assessing the outcome of the project, and by planning future products based on the present device.

3. Requirements

VHiSSI requirements were stated and agreed based on a number of use cases planned for the interface device. These use cases include a SpaceWire-to-SpaceFibre bridge, a SpaceFibre interface to an instrument, a SpaceFibre interface to on-board Mass Memory, a telemetry mode and interface to various processors, such as the general purpose LEON3FT-based dual core GR712RC space computer from Aeroflex Gaisler and Ramon Chips [2] and Ramon Chips' future high performance RC64 many-core DSP processor [3]. Requirements included data rates, formats, signaling, protocols, configuration, flexibility, programmability and networking configurations as well as technical aspects including package, voltage levels, space standards for devices such as ESCC9000 and radiation hardness levels.

4. Interface Device Architecture

Internally, the device architecture includes switching and routing functions, as well as network management functions.

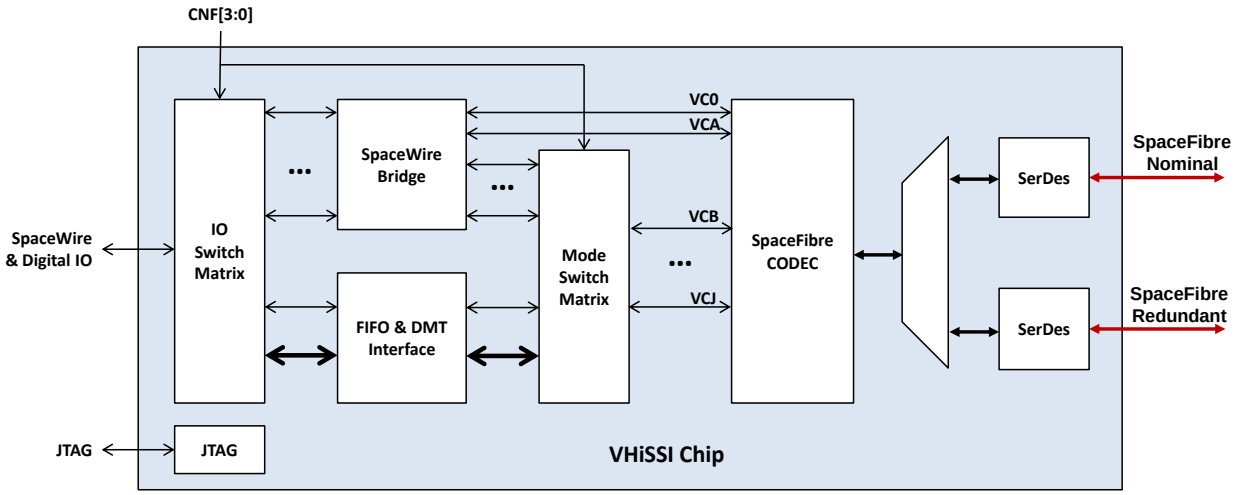

Figure 1 VHiSSI Overall Architecture

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a SpaceWire router which allows routing between SpaceWire ports and Virtual Channel (VC) buffers of the two SpaceFibre interfaces. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0 or VCA of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package. The FIFO mode provides a direct parallel interface to two SpaceFibre virtual channels. The memory type interface provides a 32-bit bus interface for accessing VHiSSI registers or VC buffers. It is a multiplexed address/data bus, with the VHiSSI device providing an internal address latch/counter to hold the register/VC buffer address. The transaction interface is similar to the memory interface, but aims to simplify software interfacing. A single address line is used to distinguish commands and status information from data. A command is written to the VHiSSI device to specify the transaction that is about to take place. For data transfer to/from a VC buffer, a read of status information provides the status of the VC buffer identified in the command. The data transfer can then take place in a burst transfer the maximum size of which is determined by the VC buffer status information. The DMA interface puts the VHiSSI chip in control of data transfers. When there is data ready to transfer, an internal DMA controller in the VHiSSI device requests control of the external data bus. Once granted it then affects the data transfer. An external address latch/counter is required, which may be implemented in an FPGA. The FIFO and DMT interface is connected to the IO Switch Matrix and to the Mode Switch Matrix. On reset the IO pins and connections to the VC buffers from the FIFO and DMT interface and SpaceWire Bridge are determined and set by these two switch matrices.

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. The other VCs have programmable VC numbers and so are referred to by letters. VCA is connected to the embedded SpaceWire router. The other VCs are either connected to the SpaceWire router, directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre

QoS which can be configured independently for each VC. VC0 and VCA are directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The other side of the SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

5. Research Challenges

This is the first time that a complex SpaceFibre system is devised and designed. The challenge is made even more complex when the requirement for very high reliability is added. The analog design is challenged by the need to achieve very high bit rate (up to 3.125 Gbps) using a relatively old technology (130nm) and accommodating very wide supply variations and very wide cabling requirements. The I/O interfaces of the device need to support multiple and conflicting electrical modes such as LVTTL and LVDS. The device must be designed for high speed while using an off-the-shelf hermetically sealed package that was not designed for high speed operation. The network management logic needs to be designed while the SpaceFibre standard proposal is still in its formative stage. New use cases are being developed as the usefulness of this device becomes clearer to architects of future on-board data processing systems.

6. Test chip

A test chip has been designed and fabricated and is presently being tested. The test chip contains the analog part of the SERDES, all I/O circuits and various logic tests.

7. Plans and future steps

The partners to this collaborative project plan to complete the design on FPGA and test it thoroughly in all use cases before casting the design in silicon. A working demonstration prototype of the chip is planned for late 2014. After the end of the funded research project, the partners plan on engaging in commercialization of the device, on final testing according to space standards, and on making it available to the European space industry by 2016.

References

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