

An Adaptive Sensitivity™ TDI CCD Sensor

Sarit Chen and Ran Ginosar

VLSI Systems Research Center
Department of Electrical Engineering
Technion - Israel Institute of Technology
Haifa 32000, Israel
sarit@tx.technion.ac.il, ran@ee.technion.ac.il

ABSTRACT

The pixel-level Adaptive Sensitivity technology enables image sensors to acquire wide dynamic range scenes without loss of detail, by adjusting the sensitivity of each individual pixel according to the intensity of light incident upon it. An Adaptive Sensitivity TDI (time delay and integrate) CCD sensor test circuit has been designed and fabricated. The sensor comprises 18 TDI integration stages, with a horizontal resolution of 32 pixels. The level of charge integrated in each pixel is monitored as the pixel charge packet progresses across the TDI array. If the charge accumulates to above a certain threshold level, the pixel is discharged. Such 'conditional reset' mechanisms are inserted after the thirteenth stage and again after the seventeenth stage. Thus, each individual pixel may be integrated over either 1, 5, or all 18 stages. Since in TDI scanning, as in all linear imaging situations, there is no concept of "frames" and each pixel is imaged only once, the intensity sensing and the decision on how long to integrate must be performed 'on the fly'. But, while in regular linear sensors the perpendicular fill factor is unlimited and complex control circuits may be placed next to the detectors, the two dimensional nature of TDI sensors presents much more demanding architectural and circuit challenges.

1. INTRODUCTION

CCD image sensors are relatively limited in their dynamic range to about 1000:1 at normal temperatures (10 bits, or 60 dB). At the same time, the luminance of natural and man-made scenes often spans a dynamic range 10-100 times as much. Thus, normal electronic acquisition is quite limited, in the sense that one image either captures the highlights of the scene or the shadows, but not both. The (simplified) response of a typical CCD image sensor is shown in Figure 1.

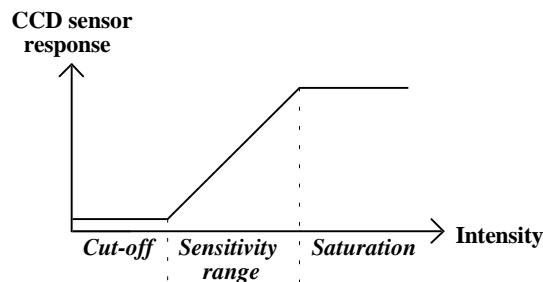


Figure 1: The response of a CCD sensor

Due to the limited dynamic range of the sensor, normal electronic acquisition is often characterized by images having some cut-off pixels and some saturated pixels, in addition to valid image pixels.

Recently we have introduced a two-dimensional *Adaptive Sensitivity (A/S)* CCD image sensor with resettable pixels and a simple off-sensor feedback mechanism which adjusts the integration time of each pixel depending on the signal level acquired by that pixel during the previous frame [1]. For example, if each pixel can integrate charge for either 1, 8, or 64 relative units of time, the sensor array as a whole achieves an increase of the total simultaneous dynamic range by 36 dB above the inherent limitations of the device.

In TDI imaging, each photoelement is replaced by a CCD shift register, which is clocked in the same rate of the image velocity. Charge is summed over the number of TDI stages available. In the A/S TDI sensor, controlling the number of charge summations is designed to assure that each pixel is operating in the linear range of the CCD response. Thus, pixels receiving low light intensity are integrated over more TDI stages, and pixels receiving high intensity levels are integrated only over a few stages, preventing them from getting saturated. In this way, the dynamic range of the entire TDI sensor is expanded.

2. SENSOR ARCHITECTURE AND OPERATION

The A/S TDI CCD sensor test chip comprises 18 integration stages, with a horizontal resolution of 32 pixels. The level of charge integrated in each pixel is monitored as the pixel charge packet progresses across the TDI array. If the charge accumulates to above a certain threshold level, the pixel is discharged. Such 'conditional reset' mechanisms are inserted after the 13th stage and again after the 17th stage. Thus, each individual pixel may be integrated over either 1, 5, or all 18 stages. The A/S TDI sensor architecture is shown in Figure 2.

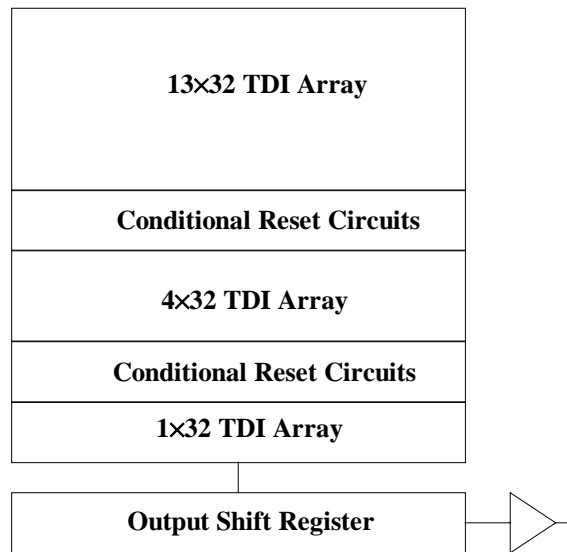


Figure 2: The A/S TDI CCD Sensor Architecture

Since in TDI scanning, as in all linear imaging situations, there is no concept of "frames" and each pixel is imaged only once, the intensity sensing and the decision on how long to integrate the pixel must be performed 'on the fly'. But, while in regular linear sensors the perpendicular fill factor is unlimited and

complex control circuits may be placed next to the detectors, the two dimensional nature of TDI sensors presents much more demanding architectural and circuit challenges.

The conditional reset circuit is based on nondestructive sensing of the pixel charge packet by the phase-four gate, which is floating in this case (see figure 3). After pre-charge to V_{gg} , the voltage on the floating gate is changed as the charge packet arrives, by ΔV_{fg} , where Q_s is the pixel charge and C_L is the gate capacitance [2]. The floating gate voltage V_{fg} is compared to the threshold voltage V_{ref} by the comparator. If V_{fg} is lower than V_{ref} (i.e. the pixel charge is too large), the output from the comparator enables the pixel discharge through the discharge gate. The inverter at the comparator output assures proper voltage levels. The reset transistor, gated by ϕ_{reset} , is added to prevent inadvertent reset as long as there is no charge under the floating gate.

The conditional reset circuits are positioned between the CCD columns. To improve the fill factor of the test chip, one such circuit is used for each two columns (so two floating gates are shorted together and averaged). Thus, in this application, controlling the exposure time is done for each two adjacent pixels and not for a single pixel, assuming that the luminance data is similar for adjacent pixels. By using more advanced technology, smaller circuits could be achieved with less effect on the sensor resolution. In figure 4, the layout of the conditional reset circuit is shown.

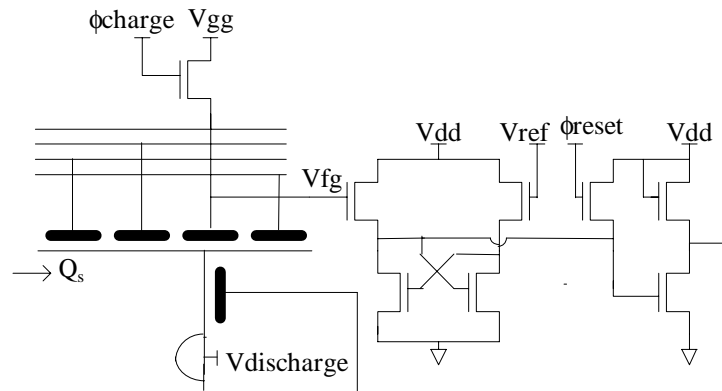


Figure 3: Conditional Reset Circuit

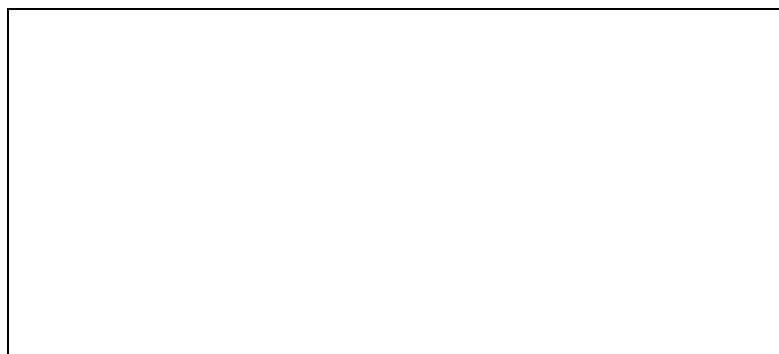


Figure 4: Conditional Reset Circuit Layout

3. TEST CHIP DESIGN AND TEST

The layout of a tiny $2.2 \times 2.2 \text{ mm}^2$ 18×32 experimental A/S TDI CCD imager test chip is shown in Figure 5. The chip was fabricated in MOSIS 2.0 micron process, with two-level polysilicon gate, two-level metal and buried n-channel CCD. Our tests have verified that most circuits perform as expected. Voltage sensing of the floating gate, however, did not prove satisfactory, and we could not discriminate different signal levels. A modified version is presently being designed.

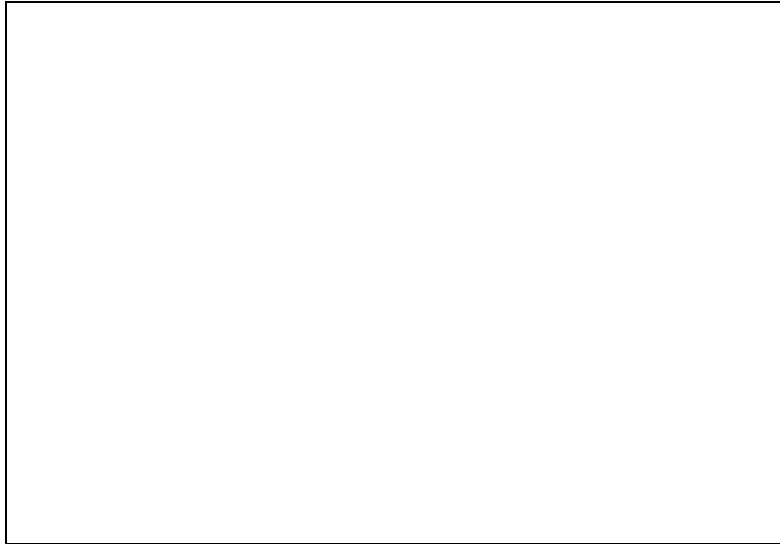


Figure 5: A/S TDI CCD Imager Test Chip Layout

4. SUMMARY

The A/S TDI CCD image sensor allows individual adjustment of the sensitivity of each pixel, independent of the other pixels. The accumulated charge is sensed 'on the fly' by means of a floating gate, affecting a conditional reset. As a consequence, the sensor can acquire a much wider dynamic range image data than is usually possible with regular TDI image sensors.

Acknowledgment: This research is funded in part by the Office of the Chief Scientist, Ministry of Trade and Commerce, and by El-Op Electro-optic Industries, Ltd.

REFERENCES

- [1] S. Chen, R. Ginosar, "Adaptive Sensitivity CCD Image Sensor", SPIE 2415: CCD and Solid State Optical Sensors V, Feb. 1995
- [2] J.D.E. Beynon and D.R. Lamb (ed.), *Charge-coupled devices and their applications*, McGraw-Hill, 1980.