# A Multichannel Recording Frontend for MEA

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**Abstract**
Glass-substrate Multi-electrode Arrays (MEAs) have become a valuable tool in neurophysiological research and drug screening. A typical setup for MEA recording is based on discrete-element preamplifiers located close to the MEA device and a multi-wire cable that conducts the pre-amplified analog signals to a data acquisition card. With the increase in the number of MEA sensing sites, this approach may turn impractical. We investigate the use of an integrated circuit as a mixed-signal analog/digital front-end for a MEA. This work presents a 0.35µm IC implementing a 12-channel mixed signal integrated front-end for neuronal recording successfully employed with a MEA system.

## 1 Conventional MEA Recording

Glass-substrate Multi-electrode Arrays (MEAs) have become a valuable tool in neurophysiological research and drug screening [1-4]. A typical setup for MEA recording (Fig. 1) is based on discrete-element preamplifiers located close to the MEA device and a multi-wire cable that conducts the pre-amplified analog signals to a data acquisition system.

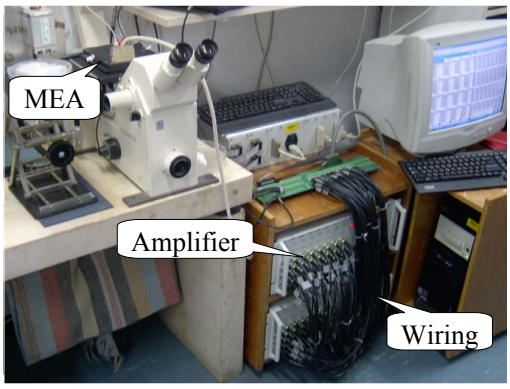


Fig.1 Laboratory MEA setup

With the increase in the number of MEA sensing sites this approach may turn impractical, due to the large number of pre-amplifying channels, data acquisition channels, and, perhaps the most important, very thick wires.

A novel approach, based on integrated circuit for MEA recording front-end, is called for. The immediate advantage is the tight integration of the analog signal conditioning and data acquisition: A single IC can handle tens of MEA channels providing a digitized data stream in a suitable format. A less obvious advantage is associated with the integration of data processing on the same die with data acquisition: A 100-channel MEA with channels sampled at 50KSps at 10-bit precision would generate a data stream of 50MSps that can be handled by a dedicated PC. A thousand MEA channels would already present a serious problem, especially if the system has to be responsive, i.e. generate stimuli as a reaction to the recorded signal. An integrated front-end with data processing capabilities can perform level detection and reduce the data-rate by sending only the segments with suspected activity. Moreover, an advanced integrated front-end may even perform spike sorting and communicate only the times and the sources of the firing events, reducing the data-rate even further.

## 2 CMOS Multichannel Neuronal Recording Frontend

### 2.1 The Frontend IC

A mixed-signal CMOS front-end chip (Fig. 2) for 12-channel neuronal signal recording was fabricated with a standard 0.35µm mixed signal CMOS process. A detailed chip description and technical discussions can be found in [5].

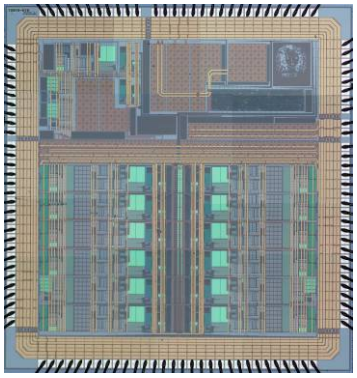

**Fig. 2** Frontend chip micrograph

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Every recording channel (Fig. 2) included an ×50 pre-amplifier with digitally programmable input signal DC nulling and single-pole band splitter, breaking the signal at around 200Hz into high frequency spike activity and low frequency local field potential. The spike part was amplified another ten times and both parts then amplified by digitally programmable variable gain amplifiers with gain settings of ×2.5 / 5 / 7.5 / 10, providing for the total of ×5000 amplification at the spike chain and ×500 amplification at the LFP chain.

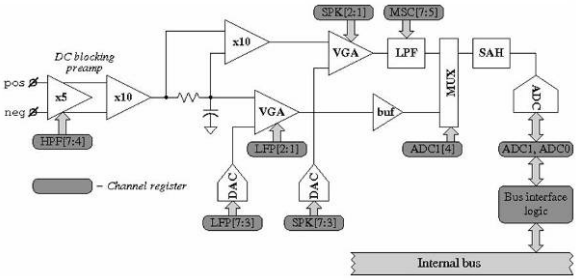


**Fig. 2** Recording channel block diagram

Digitally programmable offset calibration was provided by means of two calibration DACs at both spike and LFP chains. A sample and hold (SAH) circuit can sample either spike or LFP output and a 10-bit, successive approximation A/D converter (ADC) provides for data acquisition at every channel. Programming the various parameters is carried out by setting appropriate registers inside each channel by a host computer. The registers are accessed through an integrated parallel bus that connects all the twelve channels.

The bus is mastered by an on-chip digital controller (Fig. 3). The controller is responsible for A/D timing, channel register access, recorded data serialization and host communication. The communication is bit-serial, carried over 5-wire serial bus (McBSP). The current system is capable of providing continuous sample rates of up to 40KSps on all twelve channels, while the communication bus is running at 12.5MHz.

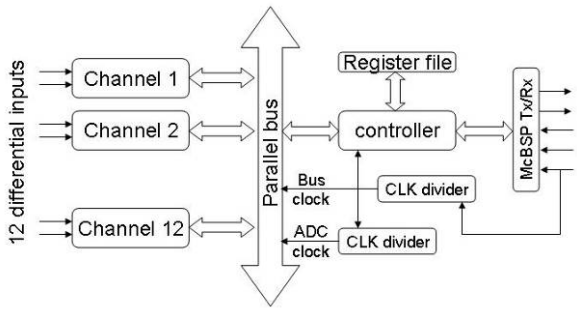


**Fig. 3** Front-end chip block diagram

An embedded FPGA board for host interface was also developed. The FPGA incorporates an Altera Nios II embedded processor running μC/II RTOS with custom developed low-level software. The interface communicates with the host over 100MBps Ethernet line, operating the UDP protocol.

## 2.2 Headstage and MEA Assembly

The front-end chip was mainly intended for in-vivo experiments; it was integrated on a miniature headstage (Fig. 4) and successfully used in in-vivo recording of rat cortical signals.

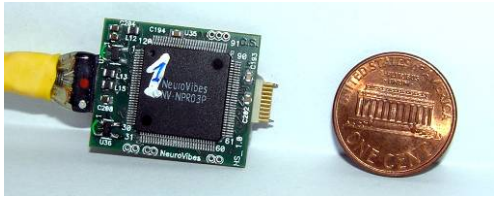

**Fig. 4** Miniature headstage (color figures are given in [6])

To couple the headstage to an MEA, a commercial MEA holder (MultiChannelSystems, Inc.) was used with the internal pre-amplifiers removed. A special adaptor PCB was designed to provide the wiring (Fig. 5).

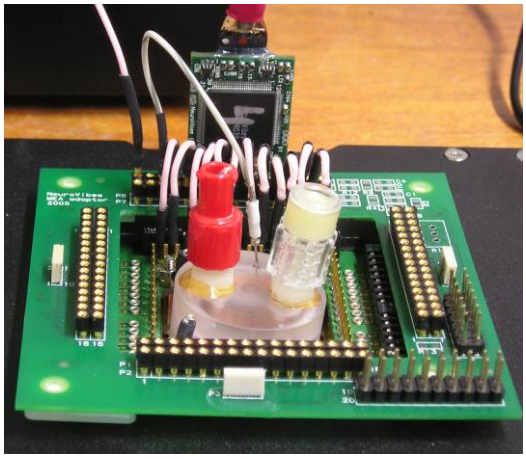

**Fig. 5** MEA, adaptor and headstage mounted on MCS MEA holder

Temperature control loop employed a commercial temperature controller with a temperature sensor and a heater within the MEA holder. Fig. 6 shows the complete assembled setup for MEA recording.

The system was tested using a standard commercial MEA with a cortical neuronal tissue. A sample signal recorded with the integrated front-end in shown in Fig. 7. A close up on a single spike is shown in Fig. 8. Signals obtained with this system are very similar to those obtained through a standard commercial signal acquisition system. Noise levels are also comparable, as demonstrated in Fig. 8. In that figure, the signals recorded from the same MEA channel by a commercial system and by the integrated front-end chip are overlaid on each other, showing that the noise levels are essentially the same and that spike levels are also similar.

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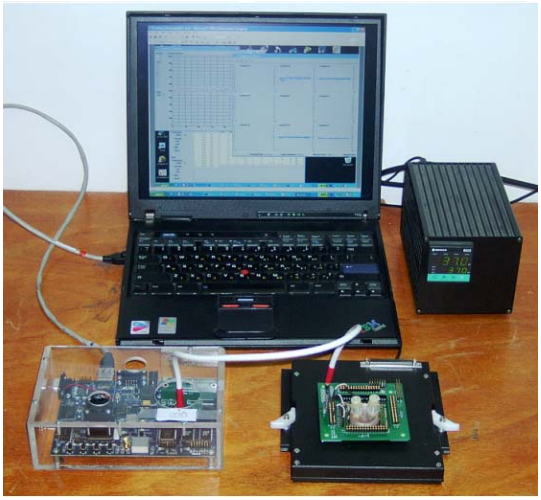

**Fig. 6** Complete MEA setup: holder with the headstage, FPGA interface board, temperature controller and host computer.

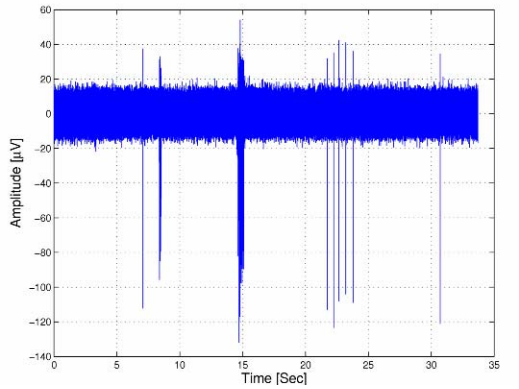


**Fig.7** Segment of a recorded signal

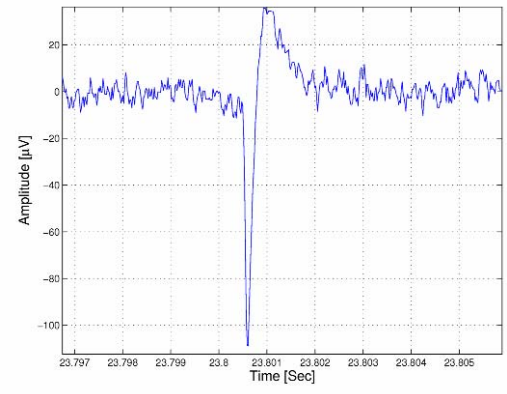


**Fig. 8** A closeup on a recorded spike

## 3 Summary

An integrated front-end was demonstrated with a standard MEA, replacing all pre-amplifiers and data acquisition circuits, thus reducing the physical size and complexity while maintaining the same signal quality. Such chips are useful for very large MEAs, enabling acquisition of thousands of channels and avoiding explosion of size, space, and power.

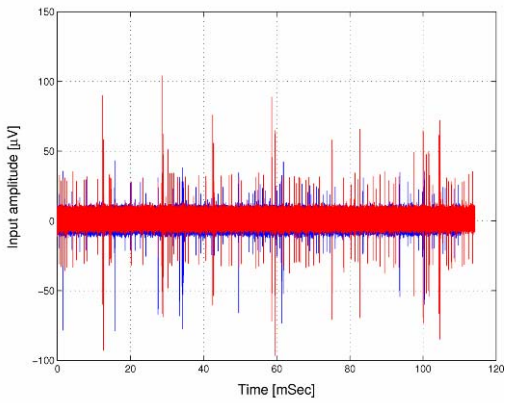


**Fig. 8** Signal recorded by the integrated front-end and signal recorded by a commercial system from the same MEA

**Acknowledgement**

We thank the staff of Neurophysiology lab, Faculty of Medicine, Technion for helping us with MEA experiments.

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