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Robust system design is essential to ensure that future systems perform correctly despite rising complexity and increasing disturbances. For coming generations of silicon technologies, several causes of hardware failures, largely benign in the past, are becoming significant at the system-level. Furthermore, emerging nanotechnologies such as carbon nanotubes are inherently highly subject to imperfections. Such Nano-Engineered Computing Systems Technologies (N3XT) are key to building transformative nanosystems since future computing demands far exceed the capabilities of today’s electronics.

Please register online: http://goo.gl/xODAS5
Advanced Circuits Research Center

Special Workshop on
Robust Nanosystems: From Today
to the N3XT 1,000X

Prof. Subasish Mitra, Stanford University
Prof. Max Shulaker, MIT

Date: 7th September 2016, 9:30-15:00
Location: Meyer building, Viterbi Faculty of Electrical Engineering, Technion, Haifa, Israel

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This workshop will address the following major robust system design goals:

1. New approaches to thorough test and validation that scale with tremendous growth in complexity. We present QED (Quick Error Detection) and Symbolic QED techniques for dramatic improvements in pre-silicon and post-silicon validation of complex System-
on-Chip (SoC) designs. Results collected using commercial hardware platforms and difficult bug scenarios demonstrate: (a) up to 9 orders of magnitude quicker detection of errors induced by bugs; (b) 4-fold improvement in improvement in bug coverage; and, (c) detection and localization of difficult bugs in only a few hours for an industrial multi-core SoC consisting of half-a-billion transistors. In contrast, traditional model checking cannot scale to such large SoCs, and traditional post-silicon debug techniques might take weeks (or months) of manual work.

2. Cost-effective tolerance and prediction of failures in hardware during system operation. Such reliability failures may be caused by radiation-induced soft errors, early-life failures, and circuit aging. We present a first of its kind framework called CLEAR (Cross-Layer Exploration for Architecting Resilience) which overcomes a major challenge in the design of digital systems that are resilient to reliability failures: achieve desired resilience targets at minimal costs (energy, power, execution time, area) by combining resilience techniques across various layers of the system stack (circuit, logic, architecture, software, algorithm). For example, CLEAR enables 50× improvement in resilience to soft errors with less than 6% energy cost and no speed impact for complex digital systems.

3. A practical way to build nanosystems that can overcome substantial inherent imperfections in emerging nanotechnologies and deliver three orders of magnitude energy efficiency improvements for future data-intensive applications. We demonstrate new nanosystems such as: (a) the first carbon nanotube microprocessor; and, (b) the first monolithically-integrated three-dimensional integrated circuits with vertically-integrated layers of logic, memory, and sensing circuits. With dense and fine-grained connectivity between vertical layers, such nanosystems capture terabytes of data from the outside world every second, and produce “processed information” by performing in-situ classification of the sensor data using on-chip accelerators designed using carbon nanotube logic.

Significant recent progress in robust system design impacts almost every aspect of future systems, from ultra-large-scale networked systems all the way to their nanoscale components.
Prof. Subhasish Mitra, Stanford University

Professor Subhasish Mitra directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University, where he is the Chambers Faculty Scholar of Engineering. Before joining Stanford, he was a Principal Engineer at Intel.

Prof. Mitra's research interests include robust systems, VLSI design, CAD, validation and test, nanosystems, and emerging neuroscience applications. His X-Compact technique for test compression has been key to cost-effective manufacturing and high-quality testing of a vast majority of electronic systems, including numerous Intel products. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools. He, jointly with his students and collaborators, demonstrated the first carbon nanotube computer, and it was featured on the cover of NATURE. The US NSF presented this work as a Research Highlight to the US Congress, and it also was highlighted as "an important, scientific breakthrough" by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, National Public Radio, New York Times, Scientific American, Time, Wall Street Journal, Washington Post, and numerous other organizations worldwide.

Prof. Mitra's honors include the Presidential Early Career Award for Scientists and Engineers from the White House, the highest US honor for early-career outstanding scientists and engineers, the ACM SIGDA/IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation, "a test of time honor" for an outstanding technical contribution, the Semiconductor Research Corporation's Technical Excellence Award, and the Intel Achievement Award, Intel’s highest corporate honor. He and his students published several award-winning papers at major venues: IEEE/ACM Design Automation Conference, IEEE International Solid-State Circuits Conference, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, Intel Design and Test Technology Conference, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford."

Prof. Mitra has served on numerous conference committees and journal editorial boards. He served on DARPA's Information Science and Technology Board as an invited member. He is a Fellow of the ACM and the IEEE.
Prof. Max Shulaker, MIT

Prof. Max Shulaker began as Assistant Professor in the Department of Electrical Engineering and Computer Science in 2016, where he leads the Nanomaterials, Nanotechnologies, and Nanosystems Group at MIT. Previously to joining MIT, he was at Stanford University where he received his B.S., Masters, and PhD in Electrical Engineering.

Prof. Shulaker's research interests include the broad area of nanosystems. His research group focuses on understanding and optimizing multi-disciplinary interactions across the entire computing stack – from low-level synthesis of nanomaterials, to fabrication processes and circuit design for emerging nanotechnologies, up to new architectures – to enable the next-generation of high-performance and energy-efficient computing systems.

His research results include the demonstration of the first carbon nanotube computer (highlighted on the cover of Nature and presented as a Research Highlight to the US Congress by the US NSF), the first digital sub-systems built entirely using carbon nanotube transistors (awarded the ISSCC Jack Raper Award for Outstanding Technology-Directions Paper), the first monolithically-integrated 3D integrated circuits combining arbitrary vertical stacking of logic and memory, the highest-performance carbon nanotube transistors to-date, and the first highly-scaled carbon nanotube transistors fabricated in a VLSI-compatible manner.