

Technical Report – Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC)

Rotem Ben Hur, Nimrod Wald, Nishil Talati, and Shahar Kvatinsky, Member, IEEE

Andrew and Erna Viterbi Faculty of Electrical Engineering
Technion – Israel Institute of Technology
Haifa 3200003, ISRAEL

Abstract-This document describes in detail the optimization problem proposed in [1].

I. LATENCY OPTIMIZATION PROBLEM

The latency optimizing problem of an in-memory Boolean function has two degrees of freedom: the locations of data and the execution time of different logic gates. The following variables are defined for each logic gate:

- $(\{R_{A_j}, C_{A_j}\}, \{R_{B_j}, C_{B_j}\}, \{R_{E_j}, C_{E_j}\})$ - Location (coordinates of memory cells) of the inputs and the output of NOR gate j .
- $(\{R_{A_k}, C_{A_k}\}, \{R_{E_k}, C_{E_k}\})$ - Location (coordinates of memory cells) of the inputs and the output of NOT gate k .
- T_i - Clock cycle in which gate i (either NOT or NOR) is executed.

Therefore, each NOR gate and each NOT gate has 7 and 5 variables, respectively.

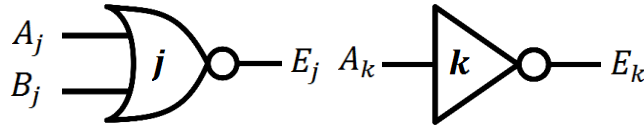


Figure 1 – Inputs and outputs of NOR and NOT gates

The execution of a given Boolean function is finished when the operations of all gates are completed, thus $\max_j(T_j)$ is the latency of a specific mapping, where $0 < j \leq \#gates$. Therefore, the latency (in clock cycles) of the best mapping is the minimum latency out of all different mappings and is

$$Latency_{best\ mapping} = \min\{\max_j T_j\}, \quad (1)$$

$$0 < j \leq \#gates$$

The legal mappings are limited by location, connectivity and timing, and are restricted by the following constraints:

1) Location constraints:

- Every input and output (I/O) has to be mapped to a memory cell, thus the coordinates of each I/O are limited by the physical size of the memory.

$$\forall x_j \in \{A_j, B_j, E_j\}: (0 < C_{x_j} \leq Col_{num}) \cap (0 < R_{x_j} \leq Row_{num})$$

- Two different outputs cannot be placed in the same memory cell (whereas the same input may be used for two different gates, therefore their inputs share coordinates). In such a configuration, reusing of a cell (after resetting) is not supported. Note that this constraint is not mandatory and is used to simplify the problem at the cost of potentially using more cells.

$$\forall E_k, E_j: (C_{E_j} \neq C_{E_k}) \cup (R_{E_j} \neq R_{E_k})$$