MTBF of a Multi-Synchronizer System on Chip

Ran Ginosar
VLSI Systems Research Center
Technion—Israel Institute of Technology, Haifa 32000, Israel
ran@ee.technion.ac.il

Summary: The MTBF of a SoC having K synchronizer is 1/K times the MTBF of a single synchronizer.

MTBF of a single synchronizer

The MTBF of a single synchronizer is known as

$$\mathrm{MTBF}(1) = \frac{e^{S/\tau}}{W \cdot F_C \cdot F_D} \qquad (1)$$

This expression is explained as follows. Define:

Failure(t)	≡	The synchronizer that became metastable at time 0 is still metastable at time t.
W	≡	Danger window during a clock cycle: If the input data to a synchronizer changes during W, then the synchronizer is assumed to have become metastable.
F_C	≡	Sampling clock frequency
T	≡	Sampling clock cycle time
F_D	≡	Frequency of changes in the input data
τ	≡	Resolution time constant of the syncnronizer

Let's assume that the input data is asynchronous relative to the synchronizer clock, and that its arrival time is uniformly distributed over the clock cycle. Given that the input data does change during a clock cycle, the probability of *entering* metastability equals the probability that the input data changes during W, namely

$$p(enter\ ms) = \frac{W}{T} = W \times F_C\,.$$

However, if input data does not change every cycle, but rather with frequency F_D, then the *rate* of entering metastability is:

$$rate(enter\ ms) = F_D \times p(enter\ ms) = W \times F_C \times F_D\,.$$

We know that, given that a synchronizer is metastable at time 0, the probability that it is still unstable at time t>0 (namely the probability of Failure(t) is

$$p[\,failure(t)\mid failure(0)] = e^{-t/\tau}$$

The probabilities of entering metastability and failure(t) are assumed independent, and thus (if data changes during a cycle)

$$p[\,failure(t)] = W \times F_C \times e^{-t/\tau}\,.$$

Given the rate of data change, the rate of failure is

$$rate[\,failure(t)] = p[\,failure(t)] \times F_D = W \times F_C \times F_D \times e^{-t/\tau}\,.$$

The MTBF, or mean time between failures, is the inverse of the failure rate. If we allot time S for settling, then the MTBF is given by Eq. (1).

MTBF of SoC having K synchronizers

Considering a SoC with K synchronizers, we say that the SoC fails if at least one of the constituent synchronizers fail. To compute that statistics, we note that

$$p(one\ synchronizer\ does\ NOT\ fail) = 1 - W \cdot F_C \cdot e^{-S/\tau}$$

The probability that all K synchronizers do not fail is

$$p(K\ synchronizers\ OK) = (1 - W \cdot F_C \cdot e^{-S/\tau})^K \approx 1 - K \cdot W \cdot F_C \cdot e^{-S/\tau}$$

The expression was simplified using Taylor expansion. Now the entire SoC fails if at least one synchronizer fails:

$$p_K[\,failure(S)] = 1 - (1 - W \cdot F_C \cdot e^{-S/\tau})^K \approx K \cdot W \cdot F_C \cdot e^{-S/\tau}$$

The rate of these failures is obtained by factoring in the data change rate, and MTBF(K) is its inverse:

$$rate_K[\,failure(S)] \approx F_D \cdot K \cdot W \cdot F_C \cdot e^{-S/\tau}$$

$$\mathrm{MTBF}(K) = \frac{1}{rate_K[\,failure(S)]} \approx \frac{e^{S/\tau}}{K \cdot W \cdot F_C \cdot F_D} = \frac{\mathrm{MTBF}(1)}{K}$$