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Citation: *Appl. Phys. Lett.* **100**, 263306 (2012); doi: 10.1063/1.4731774

View online: <http://dx.doi.org/10.1063/1.4731774>

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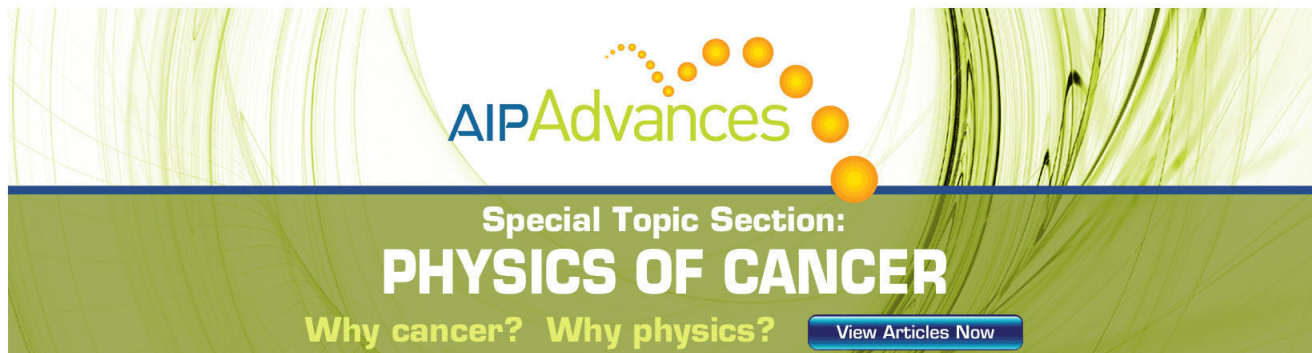
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Solution-processed ambipolar vertical organic field effect transistor

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(Received 16 May 2012; accepted 13 June 2012; published online 28 June 2012)

We report on a solution-processed ambipolar patterned-electrode vertical organic field effect transistor (PE-VOFET) based on the P(NDI2OD-T2) polymer. The Schottky barrier-based VOFET operation uniquely facilitates an ambipolar transport using a single anode-cathode-electrode and a single semiconductor material. Pin-hole free sub-100 nanometer channel length devices are obtained with no high resolution patterning owing to both the polymer's smooth morphology and the underlining patterned-electrode's flatness. The VOFET exhibits n-type on/off ratio $>10^3$, current density >50 [mAcm⁻²] under $V_{DS} = 5$ V, as well as p-type operation. Prone to design and optimization, the ambipolar PE-VOFET is a promising platform for organic complementary circuit technology. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4731774>]

Solution-processable organic field effect transistors (OFETs) attract increasing interest for low-cost, flexible, large-area electronics as their performance meets the specifications for commercial products. OFETs are expected to be integrated as the driving elements of active matrix organic light emitting diode (AMOLED) flat panel displays¹ and as the logic element for low-end off-grid applications such as smart cards and radio frequency identification tags. While in AMOLEDs, the main demand is the high current density required from the driving transistors,² logic circuits applications are based on complementary circuit technology necessary for high robustness, low power dissipation, and good noise margin.³ As in traditional silicon-based electronics, complementary logic requires the implementation of both n and p type transistors. To date, FET mobilities of unipolar organic semiconductors (SCs)—both for n and p type transport—have reached the range of ~ 1 [cm² V⁻¹ s⁻¹]. Some of these organic SCs even feature air-stable operation, extending the transistors' durability in ambient conditions.⁴ However, from a practical point of view, it is desirable that a single SC material demonstrates ambipolar transport properties and that a single device structure presents ambipolar operation together with low power consumption.

The main difficulty in achieving ambipolar OFET operation with a single SC and a single injecting electrode material does not typically reside in the intrinsic SC ambipolar transport properties but in the required low injection barriers for both holes and electrons.³ In this situation, either the holes- or electrons-injection barrier height will equal at least half the bandgap resulting in non-ohmic contact properties that hinders the low-power operation of lateral FETs. One approach to overcome this difficulty is by using two different injection electrodes⁵ or electrode materials.⁶ In this situation, one material would serve to inject holes into the SC highest occupied molecular orbital (HOMO) while the other material would serve to inject electrons to the SC lowest unoccupied molecular orbital (LUMO). Another approach is to use narrow

bandgap SCs (Refs. 7 and 8) in which the barrier is sufficiently low so as to facilitate, close to, ideal OFET characteristics. A third approach, thoroughly investigated in recent years, is the use of two SCs, such as those employed in bilayer-type⁹ or solution-processed heterogeneous blends^{3,10,11} comprising an interpenetrating network of p-type and n-type SCs—each aligned with the work function of one of the electrodes'. Here, we propose another approach to facilitate a simple and efficient ambipolar FET operation utilizing the patterned electrode vertical organic field effect transistor (PE-VOFET)¹² platform in a VOFET configuration.^{13,14}

The PE-VOFET's unique architecture (Figure 1) provides a facile method to implement short channel length devices, as the source-drain distance is simply determined by the active layer thickness—a parameter easily downscaled in fabrication.^{12,13,15} Consequently, its performance is characterized by low-power consumption and high driving current density; for example, under $V_{DS} = 3$ V, sufficient current is provided to operate same-size, commercially available OLED pixel at 1000 [Cdm⁻²]. We recently demonstrated a PE-VOFET,¹² originally suggested in Ref. 14, with tractable PE structure determined by nano-scale self-assembly—thus allowing design analysis and optimization.^{16,17} For example, it was shown that the design of the PE dictates the field strength required to switch the VOFET on, avoiding the need for a gate dielectric super capacitor—thus allowing high operation frequency. Hence, the realization of solution-

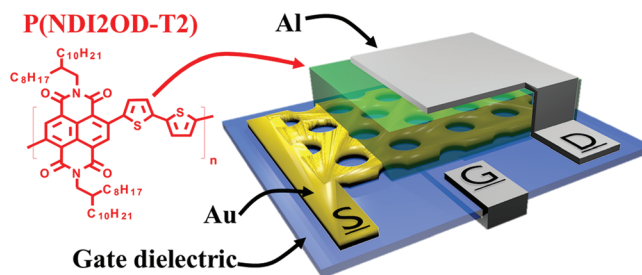


FIG. 1. Chemical structure of P(NDI2OD-T2) and 3D illustration of the PE-VOFET architecture used in this study.

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processable ambipolar patterned electrode VOFET is of great interest.

Our approach to facilitate ambipolar behavior relies on the VOFET's Schottky-based operation. As opposed to lateral OFETs, the potential barrier between the source/drain contacts and the SC is a prerequisite demand, eliminating the source-drain off currents. As a result, when the gate is unbiased, the source-drain current can be described under the field-enhanced thermionic emission theory^{16,18} as given by Eq. (1) (contact limited (CL) regime),

$$J_{\text{Off}} = \frac{q\mu_n N_0}{L(1-FF)} V_{DS} \cdot \exp\left[-q/kT\left(\phi_{b0} - \sqrt{qV_{DS}/4\pi\epsilon_0\epsilon L_{\text{eff}}}\right)\right]. \quad (1)$$

In Eq. (1), FF and ϕ_{b0} are the fill factor (the perforations area ratio) and the PE-SC potential barrier, respectively; the remaining parameters have their usual meaning. Based on this description, the potential barrier is extracted by fitting the VOFET output characteristics when the gate is unbiased (Figure 2(a), blue circles) to Eq. (1). As gate bias is applied, electric fields which penetrate through the PE perforations lowers this barrier (according to the Schottky model, $\Delta\phi = \sqrt{qF_{\perp}/4\pi\epsilon\epsilon_0}$), thus enabling efficient charge extraction into the perforations region. Saturated with mobile charge carriers, a virtual contact is formed whose physics resembles that which is found in ohmic contacts and ideally results with a space charge limited (SCL) current regime. Hence, to obtain the theoretical ON/OFF ratio, one needs to divide the expression for SCL current by that of the CL current.¹⁷ The result is shown in Eq. (2), which can be used to deduce that the PE-SC potential barrier range should be higher than 0.7 eV in order to enable a sufficiently high ON/OFF performance. Hence, to facilitate ambipolar VOFET using a single injecting electrode material (the patterned electrode behaves both as the anode and as the cathode), the SC bandgap should be at least 1.4 eV,

$$J_{\text{On}}/J_{\text{Off}} = \frac{9}{8} \frac{\epsilon_0\epsilon FF}{qN_0(1-FF)} \frac{V_{DS}}{L^2} \cdot \exp\left[q/kT\left(\phi_{b0} - \sqrt{qV_{DS}/4\pi\epsilon_0\epsilon L}\right)\right]. \quad (2)$$

To validate this approach, we fabricated PE-VOFETs using the air-stable polymer P(NDI2OD-T2) (Polyera,

ActiveInk™ N2200). This recently developed⁴ polymer has drawn significant interest,^{10,19} having promising electrical properties such as very large electron mobility in ambient⁴ as well as good ambipolarity under appropriate conditions.²⁰ Electron transport is facilitated by the sufficiently low LUMO level (~ 4 eV), which hinders charge trapping by $\text{O}_2/\text{H}_2\text{O}$.²¹ Further considerations are: the ~ 1.45 eV bandgap, the relatively high hole transport mobility, and the smooth morphology of the polymer film. This last point is significant, considering the factors limiting the reduction of the active layer thickness (the device channel length). Downscaling this, thickness is limited either by the PE roughness as in the case of the CNT VOFET (Ref. 22) (due to pinhole formation) or by the roughness of the active layer itself as in the case of the n-type fullerene (C_{60}).¹² Here, through adopting both the flat PE (Ref. 12) design and a low surface roughness solution-deposited polymer (1.5 nm),²³ downscaling the channel length to the sub 50 nm scale is achieved, further improving device power consumption.

The device fabrication protocol follows the one described previously,¹² except for the active layer deposition (prior to which the samples are placed in an inert nitrogen atmosphere glovebox). The gate and insulator are doped Si and 100 nm SiO_2 , respectively. P(NDI2OD-T2) was spin-coated from chloroform solution to the thickness of 85 nm followed by a mild annealing process at 110°C in a vacuum oven. Finally, Al top contact was thermally deposited to form the drain, resulting in the structure shown in Figure 1. Electrical analysis was carried out in the dark using SPA (Agilent 4155B).

Output and transfer n-type characteristics are shown in Figures 2(a) and 2(b), respectively. Using Eq. (1), the potential barrier extracted from the $V_G = 0$ V curve in Figure 2(a) is found to be 0.7 eV. The same equation allows us also to extract the channel length value (87 nm), in good agreement with the profilometer measurements (85 nm) carried out during the device fabrication. Figure 3 shows the ambipolar operation of the PE-VOFET device. As the bulk P(NDI2OD-T2) hole mobility is lower than that of the electrons, the power consumption in this regime is higher, requiring a higher absolute driving voltage (V_{DS}). We further note that the magnitude of the onset voltage is higher in the p type regime. This is attributed to a slightly higher barrier for hole injection (assumed to be 0.75 eV). The non-ideal off currents shown in Figure 3 are accounted for by the Al top contact,

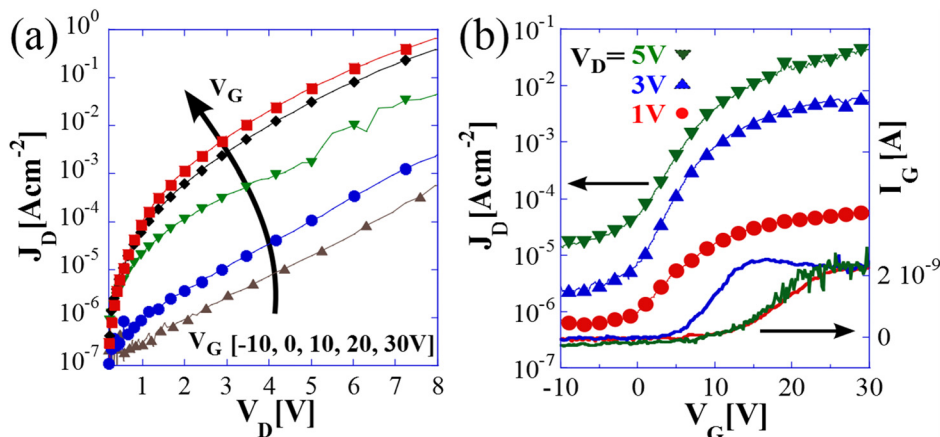


FIG. 2. (a) Output characteristics (I_D - V_D) for gate bias of [-10, 0, 10, 20, 30] V. (b) Left axis, transfer characteristics (I_D - V_G) for drain bias of [1, 3, 5] V. Right axis, gate leakage currents given in absolute values. Maximum ON/OFF is $\sim 5 \times 10^3$.

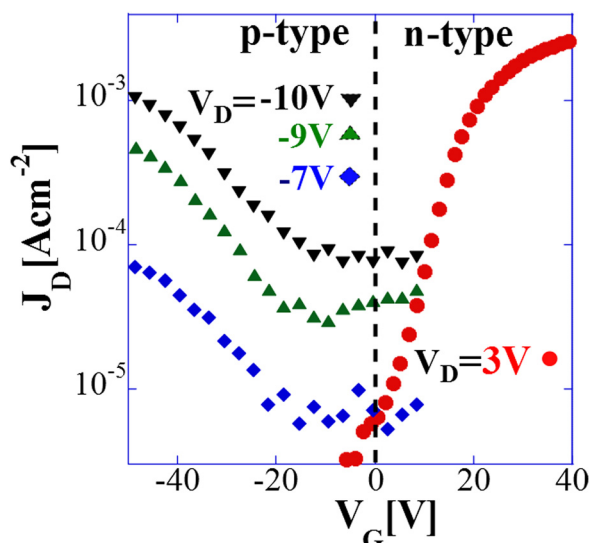


FIG. 3. Ambipolar behavior of the P(NDI2OD-T2) PE-VOFET with 85 nm channel length and 100 nm SiO₂ gate dielectric. Higher off current at the negative regime are due to electron injection from the top drain electrode.

which is better aligned with the P(NDI2OD-T2) LUMO level—facilitating electron injection from the drain. An ideal top contact would have a work function located in the bandgap center to minimize charge carrier injection of both electrons and holes. We note that the overall PE-VOFET power consumption is very low, delivering over 50 [mAc m⁻²] under applied drain-source voltage of 5 V in the n-type regime—much lower than the applied source-drain bias commonly required, particularly in single SC ambipolar OFETs.⁸ The relatively high gate voltage range required to switch the transistor on is non-correlated with the above considerations—and could be downscaled simply by increasing the gate capacitance. Figure 4 shows such an example, where the transfer characteristics of a device with 10 nm of AlO_x as

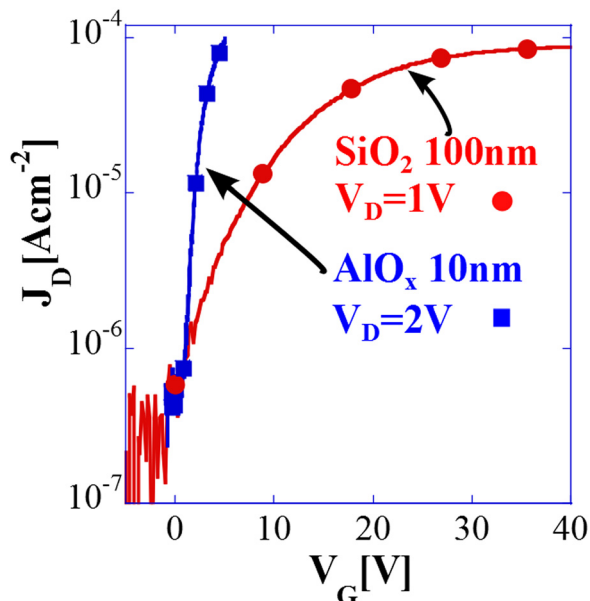


FIG. 4. Transfer characteristics comparison of PE-VOFETs with down-scaled gate dielectric (10 nm AlO_x) (blue, rectangles) and regular one (100 nm SiO₂) (red, circles).

gate dielectric demonstrate switching in a narrower range of gate bias—thus facilitating low voltage operation (<5 V).

To summarize, we have presented solution-processed ambipolar PE-VOFET. Its design is based on well-established models and optimization guidelines,^{16,17} such as those applying to the source/drain energy levels, the significance of the dielectric capacitance, and the PE geometry. The different physics underlying the behavior of the VOFET, a Schottky barrier based OFET, is exploited for the design of single anode-cathode-electrode ambipolar OFET with a single SC characterized by a bandgap (1.45 eV) larger than otherwise necessary. We consider such a design, which combines excellent performance (low-power consumption, high current density, and ambipolarity) together with simplicity of fabrication (single SC, single cathode-anode electrode, and short channel lengths) as a promising candidate for bringing efficient organic logic circuits one step closer towards demanding practical applications.

This research was supported by the Israel Science Foundation (Grant no. 695/10) and the Russell Berrie Nanotechnology Institute at the Technion—Israel Institute of Technology. Ariel J. Ben-Sasson is grateful to the Azrieli Foundation for the award of an Azrieli fellowship.

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