Organic Field Effect Transistors

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1 Introduction.

Field effect transistors (FETs) are the basis for all electronic circuits and processors, and the ability to create FETs from organic materials[1-9] raises exciting possibilities for low cost disposable electronics such as ID tags and smart barcodes. The molecular nature of organic semiconductors allows sub-micron structures to be created at low cost using new soft-lithography [10, 11] and self-assembly techniques [12] in place of expensive conventional optical lithography [3], and their emissive nature allows for optical transmission elements to be integrated directly with electronic circuits [13-16] in a way that is not possible with (non-emissive) silicon circuitry. However, although it is easy to argue for the importance of plastic FETs by drawing comparisons with silicon circuits, one must be aware that the two material systems (and the corresponding device structures) are very different, and the behaviour and performance of organic FETs do not necessarily match those of their silicon counterparts. In particular, one should not expect plastic circuits to replace silicon as the favoured

basis for electronic circuitry but one should instead look for new and emerging applications made possible by this new technology. In this chapter, we recognise that we can not take physical models developed for Si-FETs, merely substitute the text *silicon* for *organic*, and expect the existing models to apply equally well to organic devices. Instead, we will need to examine the physics of OFETs more-or-less from scratch to develop a working understanding of this new technology.

2 The Field effect transistor

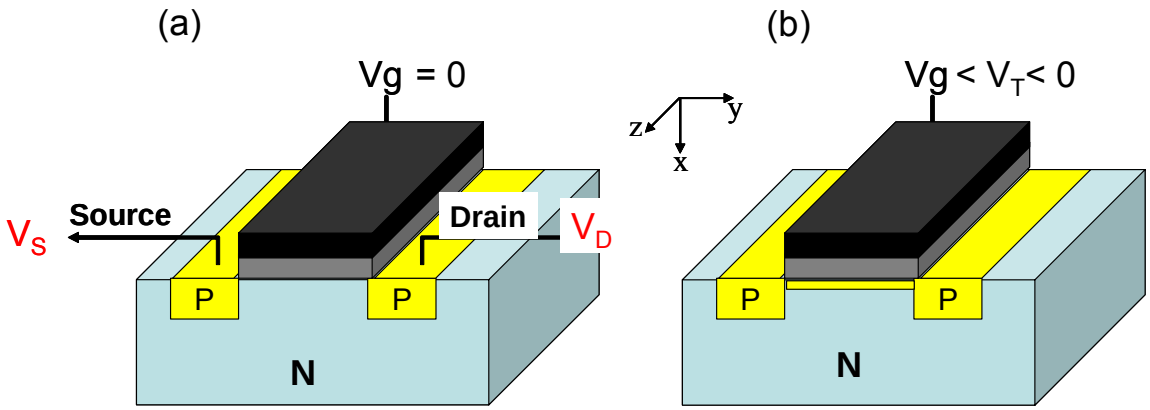

Figure 1. Schematic description of the principle of operation for "standard" semiconductor FET.

The transistor is a *three-terminal* component in which the current flow between two of the terminals – known as the *source* and *drain* – is controlled by the bias applied to the third terminal – known for obvious reasons as the *gate*. This is most simply illustrated by consideration of a conventional (inorganic) metal-oxide-semiconductor (MOS) FET as found in almost all modern circuitry. The MOSFET consists of a conductive substrate which is either negatively (N) or positively (P) doped, two electrode region (oppositely doped), and a metal-oxide double layer. The basic principle of the MOSFET is illustrated in Figure 1, where

Figure 1a and 1b show the device in its OFF- and ON-state respectively. In order to drive a current between the source and drain electrodes in the OFF-state, one has to apply a voltage (V_{DS}) across three regions: (i) a P-N junction; (ii) an N-doped bulk region; and (iii) an N-P junction. In this case, one of the junctions is always oriented in the reverse direction to the applied field and hence the current flowing through it is based on the negligible density of minority carriers (holes in N type region) making its value negligibly small. In the ON-state, a large negative bias is applied to the gate electrode. The metallic gate, the oxide layer and the N-type bulk semiconductor act in effect as a capacitor with the gate forming one plate, the oxide acting as the dielectric spacer, and the semiconductor forming the other plate. As with any capacitor, if a bias is applied across the plates, opposite and equal charges will accumulate on the two plates. Hence, electrons accumulate at the gate and holes accumulate at the oxide-semiconductor interface. If the bias applied to the gate is sufficiently high, the interfacial hole density will be large enough to change the semiconductor from N to P-type. In this case the current flowing through the reverse bias diode is enhanced due to the high density of holes in the N region. Namely, current flows between the two P-type source and drain electrodes through the intermediate P-type layer (the channel).

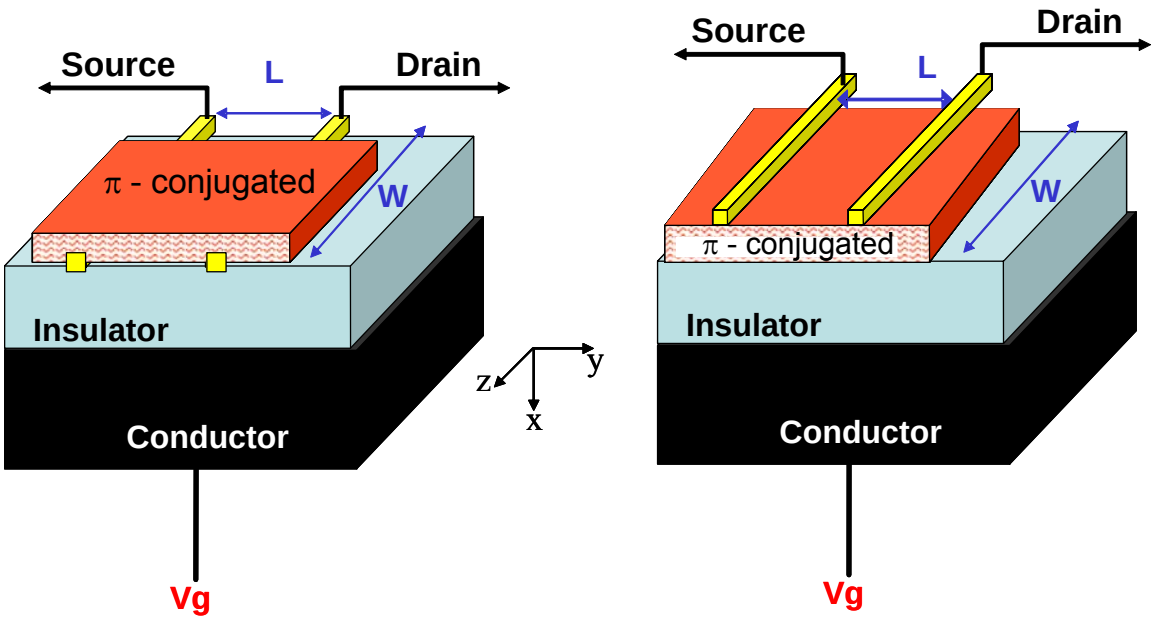

Figure 2. Schematic description of organic transistor based on Conductor, Insulator and, π-conjugated material (CIπ technology).

The basic operation of organic FETs (OFETs) and MOSFETs are in many ways similar, although there are also important differences that arise from the different device structures involved. In general OFETs comprise three parts: (i) a metal or doped-organic conductor; (ii) an insulator; and (iii) a π-conjugated semiconductor. In light of this fact, they are often described as CIπ-FETs and two typical CIπ-FET structures are shown in Figure 2. We note that, unlike the MOSFET of Figure 1, there is no P-N junction involved and the source/drain electrodes are attached directly to the π-conjugated semiconductor that makes up the channel. In Figure 2a the source/drain electrodes are in direct contact with the insulator (and the channel) and in Figure 2b the source/drain electrodes are on the other side of the π-conjugated material. These two arrangements are called *bottom contact* and *top contact* configurations respectively [17].

Before going deeply into the operation of CIπ-FET we illustrate the effect of applying the gate voltage by simulating such a device. We show in Figure 3 the charge density distribution in a top contact CIπ-FET for two gate-source bias values. The simulated structure consists of a source-drain distance (L) of 1.5μm, the π-conjugated layer thickness is 50nm and the insulator is 100nm thick. Note that at zero gate-source bias, Figure 3a, there is no charge density connecting the source and drain thus the resistance is very high as is typical of high band-gap and undoped organic materials. Once a gate bias, that exceeds a certain threshold value, is applied a high charge density is created next to the insulator interface (Figure 3b) thus significantly reducing the resistance between the source and drain. As a result, the charges (current) flow through a very thin region that it is called the "channel".

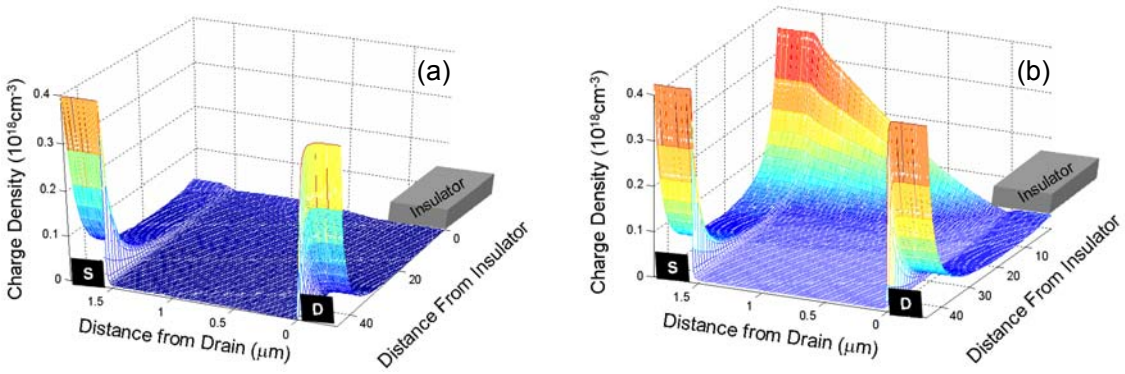

Figure 3. Simulated charge density profile for p-channel top contact CIπ-transistor V_{DS}=-1. (a) (V_{GS}-V_T)=0 (b) (V_{GS}-V_T)=-1. The figure shows the π-conjugated layer only and the position of the source drain and the insulator are schematically shown for a better orientation.

2.1 The CIπ capacitor

It is evident from the discussion above that the process of capacitive channel formation is critical to the FET operation. The capacitive effect determines the charge density in the channel and hence the threshold voltage (V_T) at which the conductivity becomes substantial (switch on). To understand the operation of CIπ-FETs, we start by considering a simple *metal-insulator-metal* parallel plate capacitor of the kind shown in Figure 4a, in which an insulating

layer is sandwiched between two metallic electrodes. In this case, the entire applied voltage is dropped across the resistive oxide layer, giving rise to a uniform bulk field of magnitude $E_{ins} = V/d_{ins}$, with no penetration of the electric field occurring into either of the electrodes (beyond the so called skin-depth). The abrupt change of the electric field from E_{ins} in the insulator to zero at the metal electrodes has its origins in the formation of vanishingly thin sheets of extremely high charge-density at the surface of the two electrodes. In the CIπ-FET one electrode is made of a semiconductor where the penetration of the electric field, which is charge density dependent, becomes more significant and hence the charge occupies a larger region near the interface. In this case, part of the applied voltage is dedicated to the formation of this charge layer (channel depth) thus reducing the voltage that drops across the insulator and consequently reducing the total charge that accumulates at the semiconductor interface (i.e. the effective capacitance is reduced).

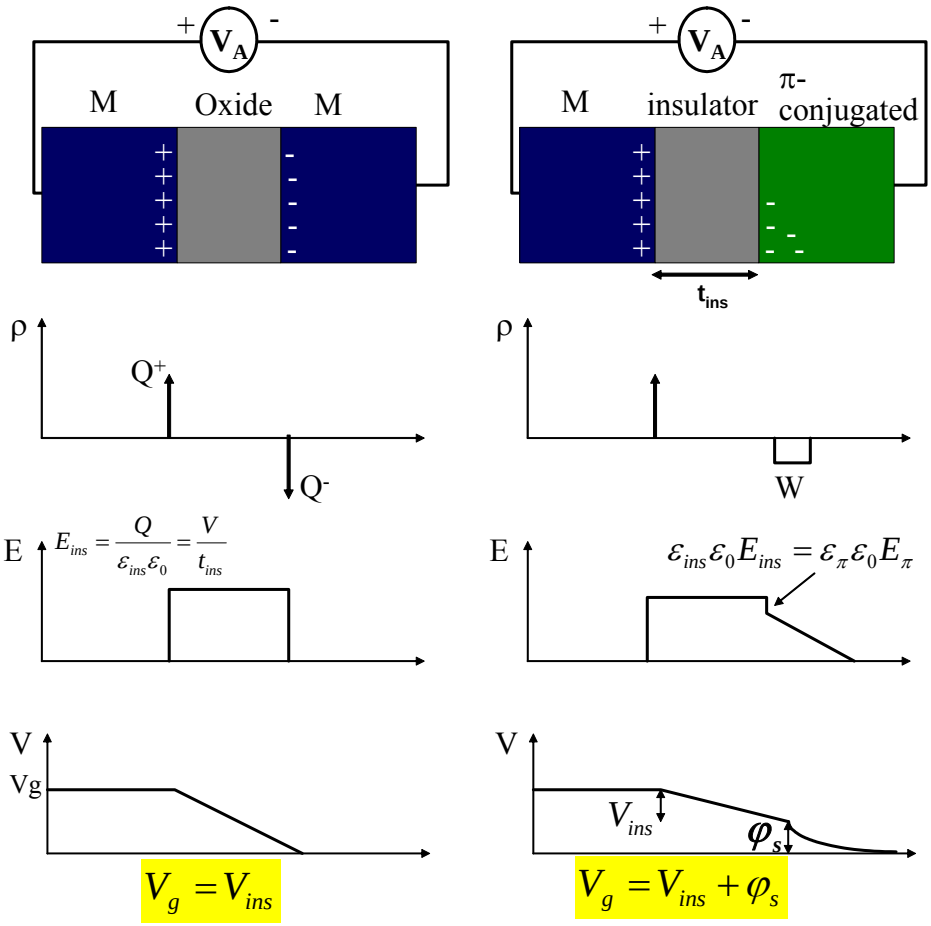

Figure 4. Schematic comparison between metal-oxide-metal and metal-oxide-semiconductor capacitors.

In the following we try to answer the question "What is the voltage required to achieve conduction between source and drain"? Or, what is the threshold voltage (V_T)? Based on Figure 1 (MOS technology)[i] it is the voltage required to invert the type of the interface from N to P. This leads us to the next question "what actually happens at the interface?" Or what is this inversion process? To answer this question we consider a doped semiconductor being part of a capacitor, Figure 5. The left column describes a P-type and the right column an N-type semiconductor, respectively. Before applying a voltage (top of Figure 5) the semiconductor is electrically neutral where every dopant atom is compensated by a free charge. When a negative (positive) bias is applied to N-type (P-type) based capacitor positive (negative) charge appears near the interface. At first it is mainly composed of dopants atoms that have been stripped of their free electron (hole).

[i] The situation CIπ technology (Figure 2) is different and will be discussed below

By depleting the free charges near the interface we create a depletion layer. When the voltage is made larger we arrive at a point where very close to the interface free holes (electrons) start to accumulate and create a very thin layer whose type has been inverted to P-type (N-type). Namely, the type of free charges at the interface is now opposite to what it was at the "no bias" state.

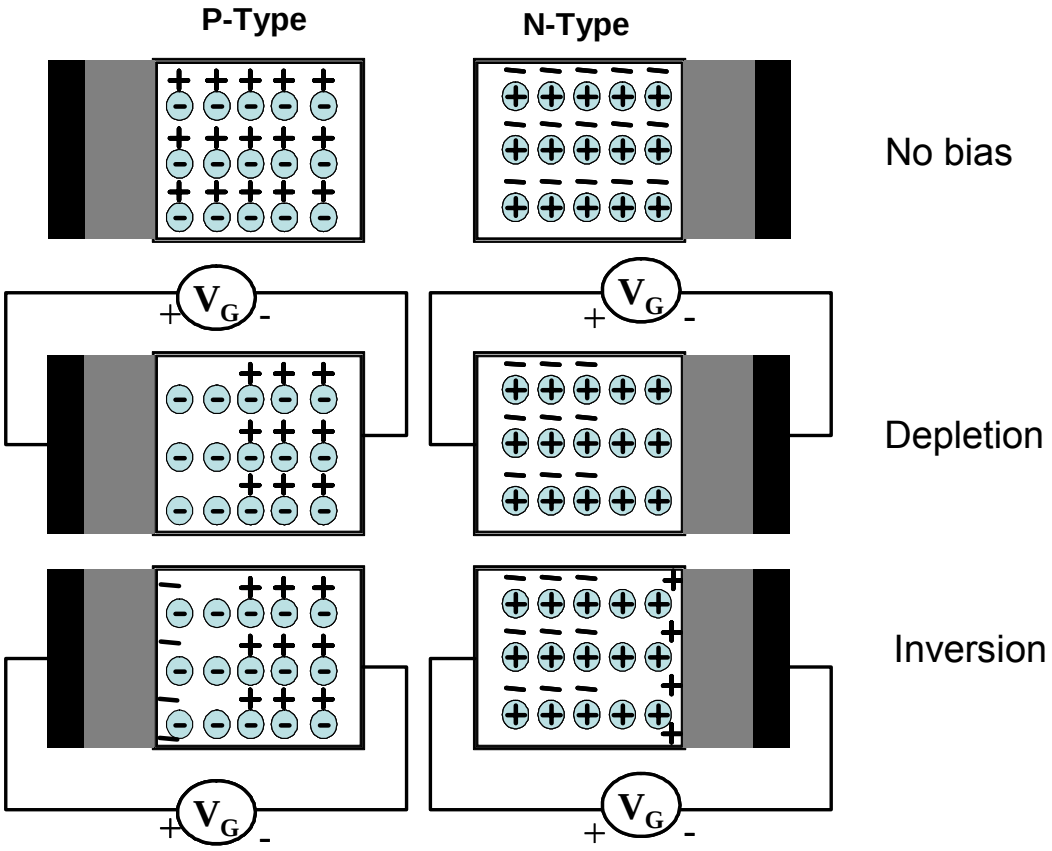

Figure 5. The formation of a depletion layer followed by inversion.

2.1.1 The role of the semiconductor parameters

How does the process of inversion depend on the material parameters? This is commonly answered with the aid of energy band diagram (Figure 6) where the position of the Fermi-level between the conduction band edge (E_C) and the valence band edge (E_V) depicts the density of electrons and holes in the semiconductor. For an intrinsic semiconductor there is an equal density (n_i) of electrons and holes and the Fermi-level lies approximately at the middle of the electronic gap. When there is an excess charge then the Fermi-level

shifts up (down) for excess of electrons (holes) and the charge density is given by $n = n_i e^{\frac{(E_F - E_{Fi})}{kT}}$ $\left(p = n_i e^{\frac{(E_{Fi} - E_F)}{kT}} \right)$, at the low density limit . In case of a metal the last (relevant) band is partially filled with electrons (high density) and the Fermi-level lies within the electronic band (see Figure 6).

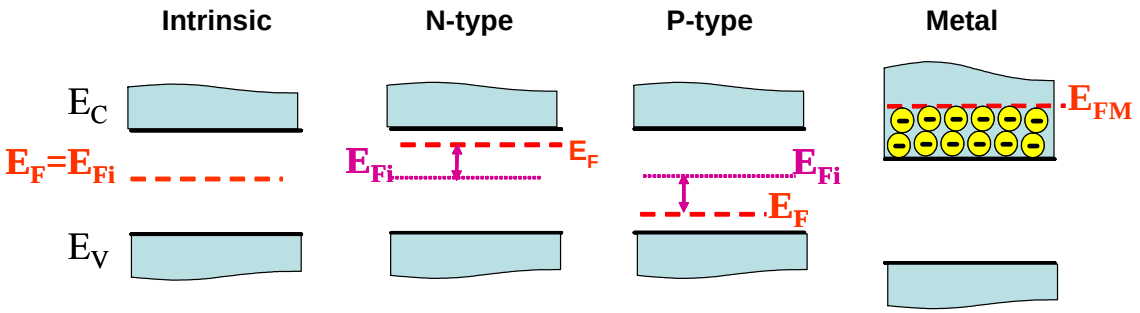

Figure 6. Schematic energy band diagram of intrinsic, N-type, and P-type semiconductors.

To invert the type of the material the Fermi-level (E_F) at the interface has to be moved to the other side of E_{Fi}, Figure 6. The voltage shift required for the inversion process is: $\left(V_{Invert} = 2 \cdot \left[E_F - E_{Fi}\right]\right)$. However, as shown in Figure 5, before inversion is created a depletion layer is formed. The creation of this space charge is associated with a voltage drop $\left(V_{Depletion} = \frac{1}{C_{ins}} \sqrt{2\varepsilon\varepsilon_0 q N_D V_{Invert}} \right)$ [18] that adds to the inversion voltage. So the threshold voltage associated with the semiconductor material only is: $V_{T\_Material} = V_{Invert} + V_{Depletion}$.

Turning now to transistors made using CIπ technology (Figure 2). What is the gate voltage required to achieve conduction between source and drain? Based on Figure 2 it is the voltage required to populate (charge) the π-conjugated layer. Typically, a well behaved CIπ-FET is made using an intrinsic (un-doped) π-conjugated layer[ii] and the Fermi level lies approximately in the middle of the HOMO-LUMO gap ($E_F \approx E_{Fi}$). Therefore, Following the above discussion we note that for an un-doped π-conjugated material there is no inversion nor depletion and $V_{T\_Material\_\pi} = 0$.

[ii] The case of doped π layer will be discussed later in the text.

2.1.2 The role of the device parameters

In the device we actually bring together a semiconductor and a metal and let them reach equilibrium through the insulating layer[iii]. As we see below, the device structure also makes a contribution to V_T. It will be remembered from §x that the Fermi level of an intrinsic semiconductor lies midway between the HOMO and the LUMO. The Fermi level of the semiconductor, as drawn in Fig. 7, therefore lies below that of the metal contact. In making an electrical connection between the organic layer and the metal, electrons will therefore flow from the metal to the semiconductor so as to bring the Fermi-level at the semiconductor up towards the metal Fermi-level; as with the single layer devices considered in §#, this creates a built in potential of $V = \Phi_M - \Phi_S$ that tilts the bands of the insulator and semiconductor upwards. The width of the spacer layer determines the potential drop across the semiconductor: in the limit $d_{ins} = \infty$ the full potential $V = \Phi_M - \Phi_S$ is dropped across the insulator whereas in the limit $d_{ins} = 0$ the full potential is dropped across the semiconductor. To restore the bands of the semiconductor (and insulator) to their flat state, one has to apply a compensating external bias of $V_{FB} = \Phi_M - \Phi_S$ [iv]. Namely, to reach a position where the threshold voltage is dependent on the material parameters we have to first apply a voltage to compensate for the effect of the structure $\left(V_{T\_Structire} = V_{FB}\right)$. The total threshold voltage is $\left(V_T = V_{T\_Structire} + V_{T\_Material}\right)$. Sometimes, during the manufacturing process charges get trapped in the insulator (charged defects) thus affecting the charge balance across the insulator and consequently the degree of band bending and the magnitude of the flat-band voltage[18].

In the discussion so far we considered that the only barrier to current flow is the lack of relevant charge carriers in the channel region. However, generally speaking there could also be a barrier at the source metal/π-layer interface. If such a barrier exists the device characteristics are distorted including an enhancement of the apparent threshold voltage.

[iii] Even when the insulator is perfect and there is no charge transfer through it the situation of common Fermi-level is achieved once an external source is applied at zero bias (short-circuit).

[iv] We assume here that Φ is given in [eV]

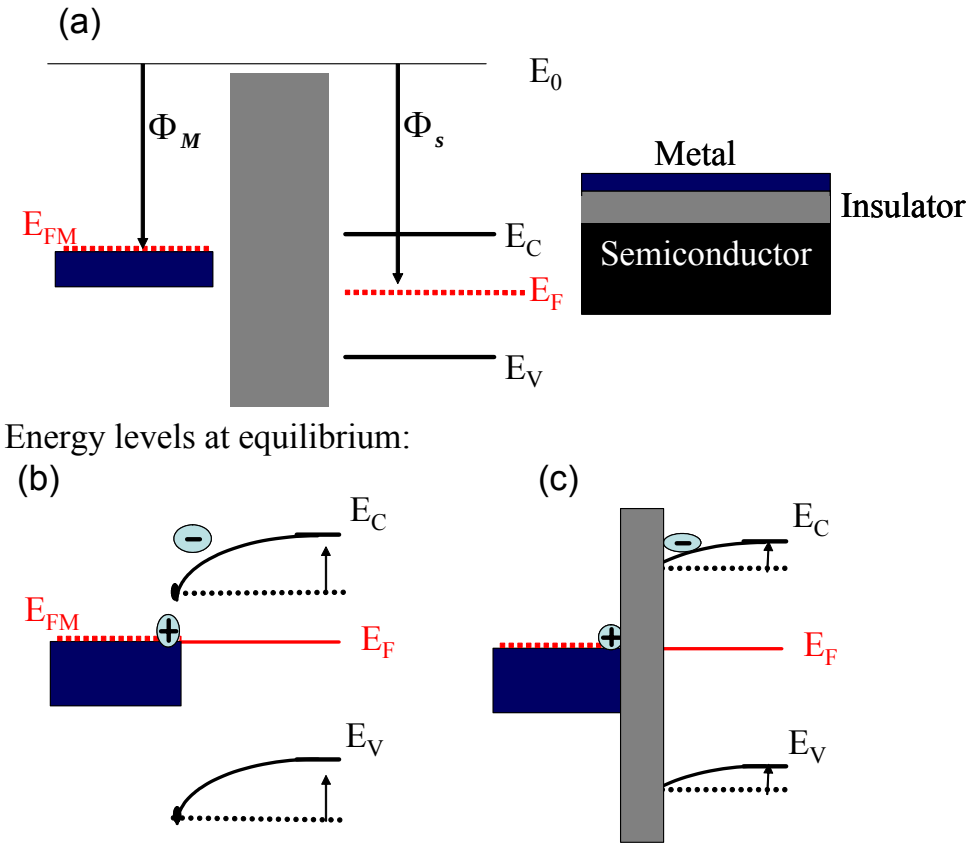

Figure 7. Band profile of a metal-insulator-semiconductor structure.

3 Possible Applications

It is early to predict where organic or CIπ field effect transistors will find their main use. It seems to be commonly accepted that they will not replace inorganic FETs but rather be used in products where inorganic transistors can not be used due to their mechanical properties or cost. Such applications could be:
1. Flexible displays where the CIπ FET is used to actively switch the pixels be them light emitting diodes or liquid crystals.
2. smart-cards or smart tags that require a relatively low density of transistors and flexibility in circuit design. Hi-end products may combine plastic circuitry with plastic displays to provide instant feedback to the user/customer.
3. The organic nature of the device may be used to better couple the device with detection capabilities of chemical or biological moieties thus making an impact also in the pharmaceutical arena.

The required performance will naturally depend on the application sought but it seems that if some logic circuitry will be used to perform a slightly complex function then it will be required that the operating voltages will be compatible with existing technologies (~5V) an that the current flowing through a single transistor will exceed several μAs to avoid noise and related errors.

4 The transistor characteristics

4.1 The linear regime

It is important to understand how the source-drain current will depend on the source-gate bias. We start by calculating the current that will flow across the channel, carried by the charge that has been accumulated by the capacitor-effect. Here we assume that the decrease of charge density along the channel is small and that the charge density is to a good approximation uniform along the channel (in the $\hat{z}$ and ŷ directions). If we assume that the transistor has the dimensions of W and L (see Figure 1) we can write the formula for the current I_{DS} that flows between source and drain as:

$$(1)\quad I_{DS} = \frac{\#Charge}{time} = \frac{Q_{Channel}\cdot(W\cdot L)}{t_{transit}}$$

where $Q_{Channel}$ is the areal charge density in the channel and $t_{transit}$ is the time it takes a charge to move across the channel between the source and drain electrodes. If we assume that the electron velocity is characterised by a constant mobility (μ) we can calculate the transit time as:

$$(2)\quad t_{transit} = \frac{L}{v} = \frac{L}{\mu E} = \frac{L}{\mu\frac{-V_{DS}}{L}} = -\frac{L^2}{\mu V_{DS}}$$

The charge area density ($Q_{Channel}$) can be found from the capacitor characteristics assuming that φ_s (Figure 4) is bias independent and is fixed at its value for $V_{GS}=V_T$ $\left(\varphi_s\big|_{V_G=V_T} = V_{Invert}\right)$. For undoped π-layer this is equivalent to the assumption that φ_s is negligible since for intrinsic layer $V_{Invert}=0$.

$$(3)\quad Q_{channel} = -C_{ins}\left(V_{GS}-V_T\right)$$

and finally we arrive at the expression for the current:

$$I = \frac{C_{ins}\left(V_{GS}-V_T\right)\cdot W\cdot L}{\frac{L^2}{\mu V_{DS}}} \quad \Rightarrow$$

(4) $I_{DS} = \frac{W}{L}\mu C_{ins}\left(V_{GS} - V_T\right)V_{DS}$

One can also derive the device resistivity in its on state

$R_{ON} = \frac{V_{DS}}{I_{DS}} = \left[\frac{W}{L}\mu C_{ins}\left(V_{GS} - V_T\right)\right]^{-1}$ and we find it is a trans-resistor (hence transistor). As equation (4) represents a linear relation between the current and voltage the regime for which it holds is called the "linear regime".

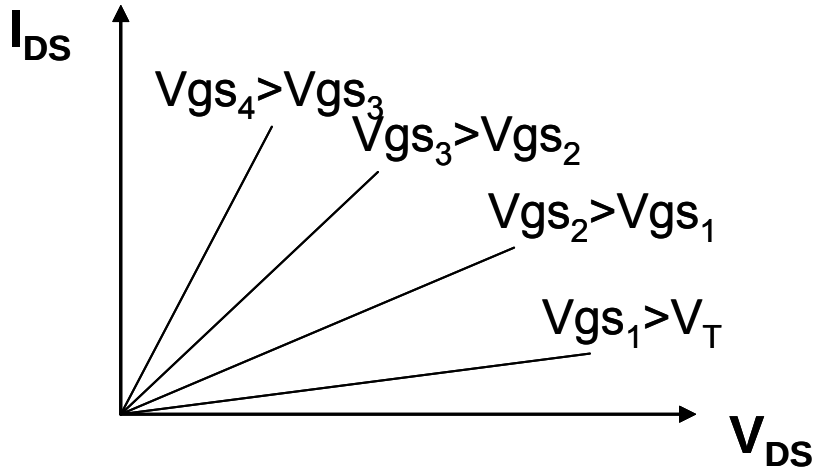

Figure 8. Schematic description of the I-V characteristics in the linear regime.

4.2 The non-linear regime and the saturation effect

The transistor is said to operate outside the linear regime when the main assumption underlying the linear regime (quasi-uniform charge density across the channel) breaks. Figure 9 shows schematically the charge distribution across the transistor channel for fixed gate (-5V) and source (0V) voltage and a varying drain (0, -3, -5, -7V) voltage. As long as the bias between gate and source and between gate and drain are similar one can assume the charge density to be relatively uniform across the channel. Namely, for $|V_{DS}| << |V_{GS}|$ the transistor is said to be in the linear regime. When V_{DS} approaches V_{GS} the formula for the current has to be re-evaluated.

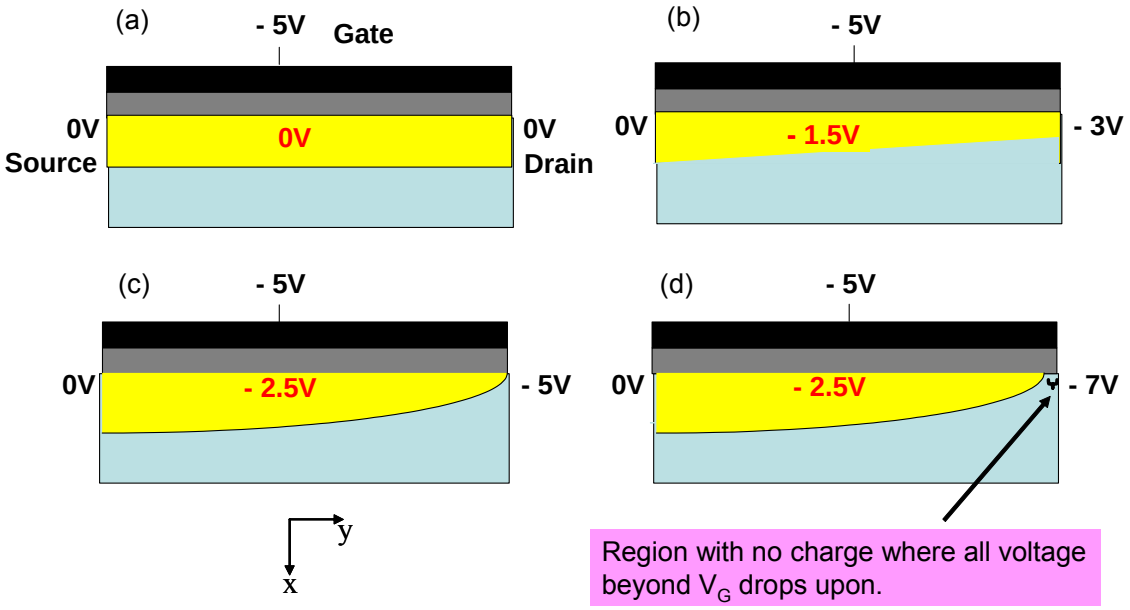

Figure 9. Schematic description of the charge density across the channel for different Drain voltage (V_G= -5, V_S=0). The thickness of the yellow line is used to denote the charge density at the channel. (a) V_{DS}=0 and the charge density is uniform across the cgannel. (b) $|V_{DS}|<|V_{GS}|$ and the charge density only slightly change across the channel. (c) $V_{DS}=V_{GS}$ and the charge density next to the drain contact is zero (d) $|V_{DS}|>|V_{GS}|$ a small region empty of charge develops near the drain electrode and the channel length is slightly reduced.

Before formally deriving the transistor I-V curve let us examine the effect of V_{DS} as depicted in Figure 9. The charge density at the channel is proportional to the potential difference between the channel and the gate (Q=CV). As was discussed in previous sections the non zero threshold voltage $V_T \neq 0$ is associated with Fermi Level alignment and charge accumulation at V=0. Therefore the actual charge that accumulates at the insulator/organic interface is the sum of that found at V=0 and that induced by the external voltage - $Q = CV - CV_T = C(V - V_T)$. The potential across the channel is set by two boundary conditions at the source (V_S) and at the drain (V_D). As V_D approaches (V_G-V_T) the charge density near the drain is reduced (Q_D=C[V_D-(V_G-V_T)]< C[V_S-(V_G-V_T)]=Q_S) thus enhancing the resistivity of the channel. When this effect takes place the slope of the I-V curve is reduced (higher resistivity) and the curve starts to saturate. Once V_D is equal to V_G-V_T a region empty of the channel type carriers is formed. When the value of V_D crosses V_G-V_T the size of this "empty" region is enhanced. Since this region is "empty" of channel type carriers its resistivity is very high and the entire extra potential drops

across this region[v] and the potential at the edge of the channel is pinned at V_G-V_T. Namely, the region where the channel exists remains with the boundary conditions of V_S on one side and (V_G-V_T) on the other for any V_D that exceeds (V_G-V_T). As the resistance per unit length is high the length of this empty region can be very small and still provide the required resistivity to accommodate the excess potential drop. Since once V_D exceeds (V_G-V_T) the boundary conditions of the channel region is fixed the current that will flow across the channel will become independent of V_D. The resulting curve will be as is shown in Figure 10.

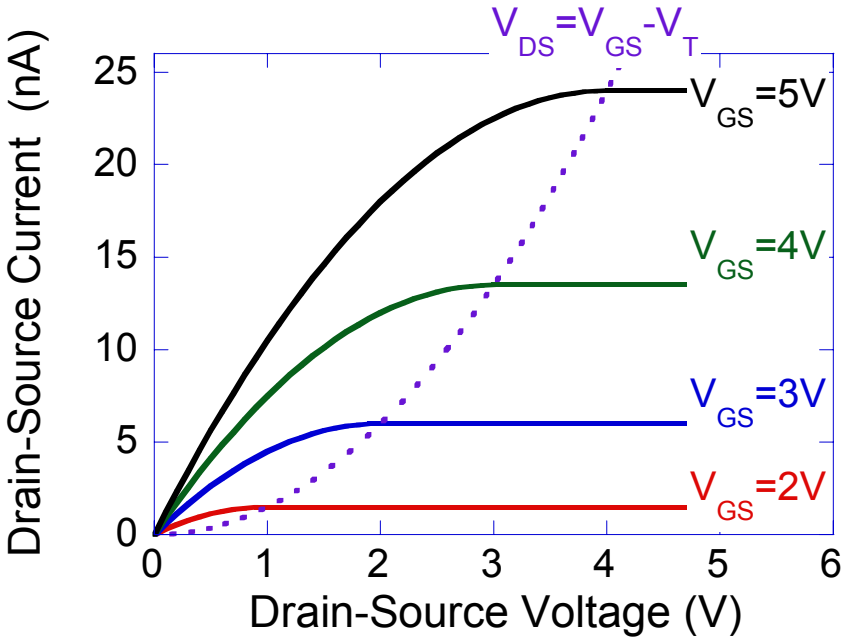

Figure 10. N-type transistor I_{DS}-V_{DS} characteristics for several values of V_{GS} as derived by equations (10) and (12) . Here, W/L=600, C_{ins}=50nF, $\mu=10^{-4}cm^2v^{-1}s^{-1}$ and V_T=1V. The dashed line depicts the transition from linear to saturation regimes.

To derive the I-V curve formally we recall that the charge is not uniform across the channel and in reality decreases rapidly from the start to the end of the channel (see Fig. 3). Accordingly we write $Q_{channel} = Q_{channel}(y)$ and its value is:

(5) $$Q_{channel}(y) = -C_{ins}\left[\left(V_G - V(y)\right) - V_T\right]$$

[v] In principle the region that is empty of channel-type carriers (hole or electron) may be filled with the other type of carrier (electron or hole). We assume that the conductivity associated with this other-type carrier is negligibly small (low mobility, contact limited, ….).

where V(y) is the electrochemical potential in the channel at point y and $\left[V_G-\left(V(y)+V_T\right)\right]$ is the voltage that drops across the insulator. Before proceeding we first show that, even in this case where charge gradient along the channel is inherent, the current in a conventional transistor is mainly drift current. To do so we write the expressions for the drift and diffusion currents:

$$\mu EN=\mu\frac{V(y_2)-V(y_1)}{y_1-y_2}\cdot\frac{N(y_1)+N(y_2)}{2}$$

$$D\frac{\partial N}{\partial y}=D\frac{N(y_1)-N(y_2)}{y_1-y_2}$$

Inserting equation (5) :

$$\mu EN=\mu\frac{V(y_2)-V(y_1)}{y_1-y_2}\cdot C^1q^{-1}\left\{V_G-\frac{V(y_1)+V(y_2)}{2}-V_T\right\}$$

$$D\frac{\partial N}{\partial y}=\frac{kT}{q}\mu Cq^{-1}\frac{V(y_1)-V(y_2)}{y_1-y_2}$$

And finally the ratio between the two currents is:

$$(6)\quad \left\|\frac{\mu EN}{D\frac{\partial N}{\partial y}}\right\|\approx\left\|\frac{V_G-V(y)-V_T}{\frac{kT}{q}}\right\|$$

Equation (6) shows that as long as the voltage drop across the insulator is larger then kT/q the current is mainly drift current and hence we can write:

$$(7)\quad I_{DS}=I_{DS}(y)=W\mu Q_{channel}(y)E(y)=W\mu Q_{channel}(y)\frac{-dV(y)}{dy}$$

Integrating across the channel we find:

$$(8)\quad \int_0^L I_{DS}dy=\int_0^L W\mu Q_{channel}(y)\frac{-dV(y)}{dy}dy$$

If $\left|V_D\right|\le\left|V_G\right|$ (Figure 9a to Figure 9c) we can replace the integration between y=0 and y=L to an integration between V(0)=0 and V(L)=V_D.

$$(9)\quad \int_0^L W\mu Q_{channel}(y)\frac{-dV(y)}{dy}dy=\int_0^{V_D} W\mu C_{ins}\left[\left(V_G-V\right)-V_T\right]dV$$

and as the current is constant:

$$I_{DS}L = W\mu C_{ins}\left[\left(V_G - V_T\right)V - \frac{V^2}{2}\right]\Bigg|_0^{V_D}$$

and finally

(10) $I_{DS} = \frac{W}{L}\mu C_{ins}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$ for V_{GS} in accumulation regime and

$\left|V_{DS}\right| \le \left|V_{GS}\right|$

In the above we have assumed that: a) there is charge in the channel anywhere between y=0 and y=L and that b) V_S and V_D can be used as the two boundary conditions for the channel (see Figure 9). Assumption b) is true as long as the contacts are ideal and no (or negligible) voltage drops across them. Assumption a) is true as long as $\left|V_{DS}\right| \le \left|V_{GS}\right|$ however, when the magnitude of V_{DS} exceeds that of V_{GS} a region empty of charge is created near the drain electrode (see Figure 9). In this case equation (8) has to be rewritten:

(11) $\int_0^{L_{EFF}} I_{DS}dy = \int_0^{L_{EFF}} W\mu Q_{channel}(y)\frac{-dV(y)}{dy}dy$ where $L_{EFF} \le L$.

And equation (9) turns into

$$\int_0^{L_{EFF}} W\mu Q_{channel}(y)\frac{-dV(y)}{dy}dy = \int_0^{V_G} W\mu C_{ins}\left[\left(V_G - V\right) - V_T\right]dV$$

and finally

(12) $I_{DS\_SAT} = \frac{W}{L_{EFF}}\mu C_{ins}\left[V_G - V_T\right]^2$ for V_{GS} in accumulation regime and $\left|V_{DS}\right| \ge \left|V_{GS}\right|$

Since the region that is empty of charge has high resistivity it can accommodate relatively high voltage across a short distance. In typical transistors this region, $\left(L - L_{EFF}\right)$, is small compared to the geometrical channel length (L) and one can approximate L_{EFF} as $\left(L_{EFF} \cong L\right)$. This approximation breaks for short channel transistor (as will be briefly discussed later).

Finally, the FET that we have discussed above is extensively used in electrical circuits and when it is placed in such a circuit design-sheet it is drawn using the symbol shown in Figure 11.

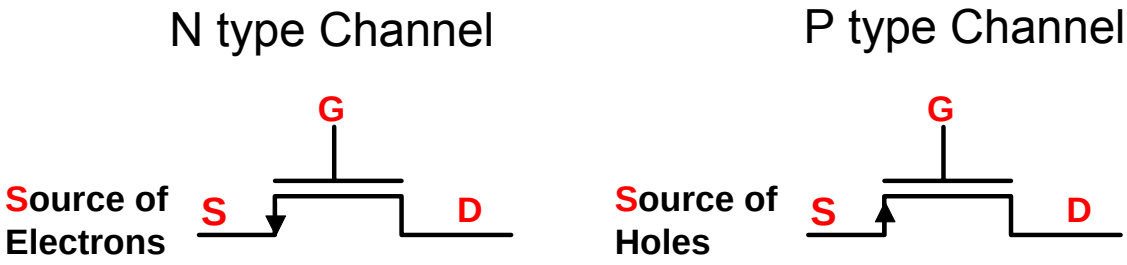

Figure 11. The electrical symbol describing N and P channel FETs.

5 Extracting Material Parameters of CIπ-FET

5.1 Field effect Mobility

If the current flowing through the transistor at hand is only affected by the transistor channel then its I-V characteristics should follow equations (10) and (12) . Namely:

$$(13)\quad \mu = \begin{cases} \dfrac{I_{DS}}{\dfrac{W}{L}C_{ins}\left[\left(V_{GS}-V_T\right)V_{DS}-\dfrac{V_{DS}^2}{2}\right]} & \textit{Linear regime} \\ \dfrac{I_{DS\_SAT}}{\dfrac{W}{L_{EFF}}C_{ins}\left[Vg-V_T\right]^2} & \textit{Saturation regime} \end{cases}$$

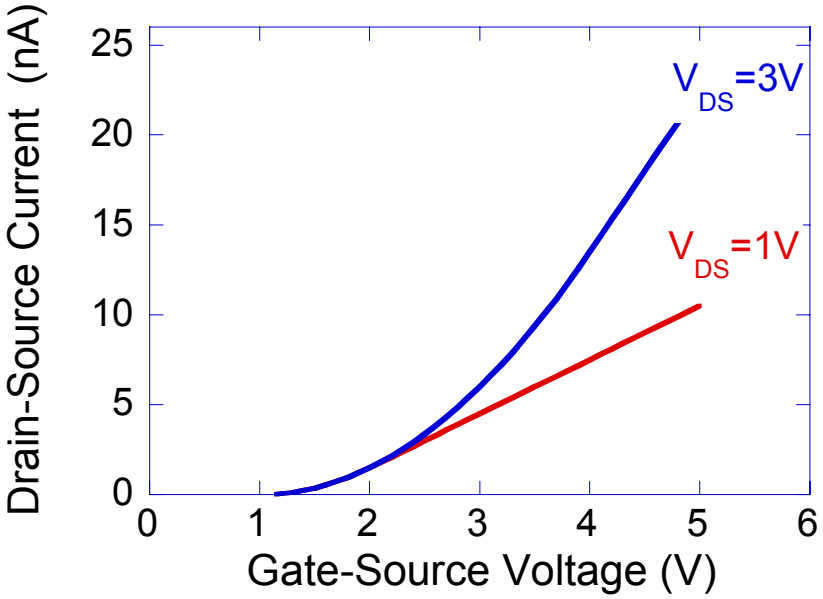

Figure 12. Calculated (using equations (10) and (12)) I_{DS}-V_{GS} characteristics of N-channel transistor for several values of V_{DS}. Here, W/L=600, C_{ins}=50nF, μ=$10^{-4}cm^2v^{-1}s^{-1}$ and V_T=1V

Sometimes it is useful to use the derivative of the above equations. For example, in the linear regime:

$$(14)\quad \frac{\partial}{\partial V_{GS}}I_{DS}=\frac{\partial}{\partial V_{GS}}\left(\frac{W}{L}\mu C_{ins}\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right]\right)$$

Applying the derivation:

$$(15)\quad \frac{\partial}{\partial V_{GS}}I_{DS}=\frac{\partial\mu}{\partial V_{GS}}\left(\frac{W}{L}C_{ins}\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right]\right)+\mu\left(\frac{W}{L}C_{ins}V_{DS}\right)$$

in cases were the mobility is independent of the gate bias (or charge density) equation (15) reduces to:

$$(16)\quad \mu = \frac{\frac{\partial}{\partial V_{GS}} I_{DS}}{\left(\frac{W}{L} C_{ins} V_{DS}\right)}$$

And the mobility is proportional to the slope of the curve in Figure 12 in the regime where it is linear. The advantage of (16) is that it is independent of V_T and hence is not prone to errors in extracting the threshold voltage however, the first term in (15) is often non-negligible in amorphous organic materials.

5.2 Background doping

The above discussion assumed that the π-conjugated layer is undoped and hence, its conductivity is zero unless charged (populated) by the applied gate-source bias. In some cases there exists a doping density in the π-conjugated layer be it intentional or unintentional [19, 20]. In such a case there would be finite conductivity between the source and drain electrodes which is associated with the bulk conductivity of the π-conjugated layer and is electrically in parallel with the channel conductivity.

$$(17)\quad I_{DS\_Bulk} = qN_D \frac{W}{L} \mu d_\pi V_{DS}$$

Here N_D is the bulk doping density, d_π is the π-conjugated layer thickness and the rest have their usual meaning. If we assume that the transistor shown in Figure 12 has now a doping density of $N_D=10^{16}cm^{-3}$ then it characteristics are as shown in Figure 13.

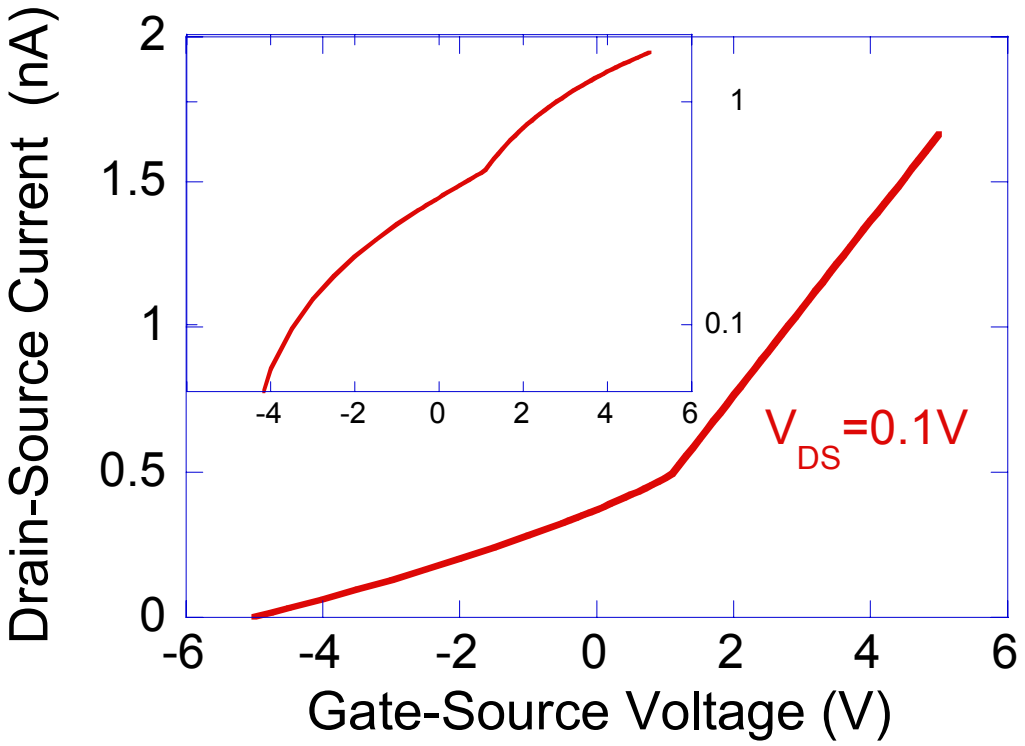

Figure 13. Calculated (using equations (10) , (12) and (24)) I_{DS}-V_{GS} characteristics of doped N-channel transistor V_{DS}=0.1V. Here, $N_D=5\cdot10^{16}cm^{-3}$, W/L=600, C_{ins}=50nF, $\mu=10^{-4}cm^2v^{-1}s^{-1}$ and V_T=1V; $\varepsilon_{ins}=\varepsilon_\pi$=2.25; $d_{ins}=d_\pi$=100nm. The inset shows the same data on log scale.

We note that for $V_{GS} > V_T$ (V_{GS}>1V) the curves in Figure 13 are similar to those in Figure 12 but are shifted upward by I_{DS_Bulk} which according to equation (17) is independent of V_{GS} (V_{DS} = 0.1V). For (V_{GS} - V_T) < 0 we note that the current is decreasing indicating the reduction in the bulk related current (as the channel is in OFF state for all $V_{GS} < V_T$). The reduced conductivity of the bulk is associated with the formation of a depletion layer similar to that shown in Figure 4 reducing the conducting layer thickness to (d_π-W_{dep}). Following the notation in Figure 4 we move to formally derive the bulk current and we write:

$$(18)\quad V=\left(E_{ins}d_{ins}+\frac{1}{2}E_{\max}W_{dep}\right)=\left(\frac{\varepsilon_\pi}{\varepsilon_{ins}}E_{\max}d_{ins}+\frac{1}{2}E_{\max}W_{dep}\right)$$

Solving for E_{max}:

$$(19)\quad E_{\max}=\frac{V}{\left(\frac{\varepsilon_\pi}{\varepsilon_{ins}}d_{ins}+\frac{1}{2}W_{dep}\right)}$$

Since the electric field decrease linearly across W_{dep}:

(20) $$E_{\max} = \frac{qN_D}{\varepsilon_\pi \varepsilon_0} W_{dep}$$

Using equations (19) and (20) :

(21) $$W_{dep} = E_{\max} \frac{\varepsilon_\pi \varepsilon_0}{qN_D} = \frac{V}{\left(\frac{\varepsilon_\pi}{\varepsilon_{ins}} d_{ins} + \frac{1}{2} W_{dep} \right)} \frac{\varepsilon_\pi \varepsilon_0}{qN_D}$$

and rearranging the terms we arrive at:

(22) $$\frac{1}{2} W_{dep}^2 + \frac{\varepsilon_\pi}{\varepsilon_{ins}} d_{ins} W_{dep} - V \frac{\varepsilon_\pi \varepsilon_0}{qN_D} = 0$$

with the only physical solution being:

(23) $$W_{dep} = \begin{cases} -\frac{\varepsilon_\pi}{\varepsilon_{ins}} d_{ins} + \sqrt{\left(\frac{\varepsilon_\pi}{\varepsilon_{ins}} d_{ins} \right)^2 + 2V \frac{\varepsilon_\pi \varepsilon_0}{qN_D}} & V < 0 \\ 0 & V \geq 0 \end{cases}$$

If we assume that V_{DS} is relatively small so that we can assume V, and hence W_{dep}, to be uniform across the device ($V=V_{GS}-V_T$):

(24) $$I_{DS\_Bulk} = qN_D \frac{W}{L} \mu \left(d_\pi - W_{dep} \right) V_{DS}$$

We observe that the current drops to zero once the depletion layer extends across the entire π-conjugated layer. If we know the voltage at which it happens we can use equations (18) and (20) to derive the dopant density ($W_{dep}=d\pi$).

$$N_D = \frac{2V_{pinch}\varepsilon_0}{q\left(\frac{d_\pi^2}{\varepsilon_\pi} + \frac{2d_\pi d_{ins}}{\varepsilon_{ins}} \right)}$$

For example, based on Figure 13 we find $V_{pinch} = V_{GS}\big|_{I_{DS}=0} - V_T = -6V$ and hence

$$N_D = \frac{2 \cdot 6 \cdot 8.85 \cdot 10^{-14}}{1.6 \cdot 10^{-19} \left(\frac{\left(100 \cdot 10^{-7}\right)^2}{2.25} + \frac{2 \cdot 100 \cdot 10^{-7} \cdot 100 \cdot 10^{-7}}{2.25} \right)} = 4.98 \cdot 10^{16} [cm^{-3}]$$

A more comprehensive treatment of doped devices that includes the effect of non-uniform W_{dep} can be found in [19].

6 Advanced Topics

6.1 The channel depth

In the development of the I-V characteristics above we did not consider the charge density profile along the x-axis, Figure 14. This was justified by the assumption we made for equation (3) that φ_s (see Figure 4) is constant once the transistor is above threshold. In other words, we neglected any changes in the charge profile and the associated change in the voltage drop across it. Adding this effect rigorously will significantly complicate the expressions as for each point along the y axis there exist a different effective capacitance and $C_{Ins} \Rightarrow C_{Ins\_EFF} = C_{Ins\_EFF}(V_{GS}, y)$.

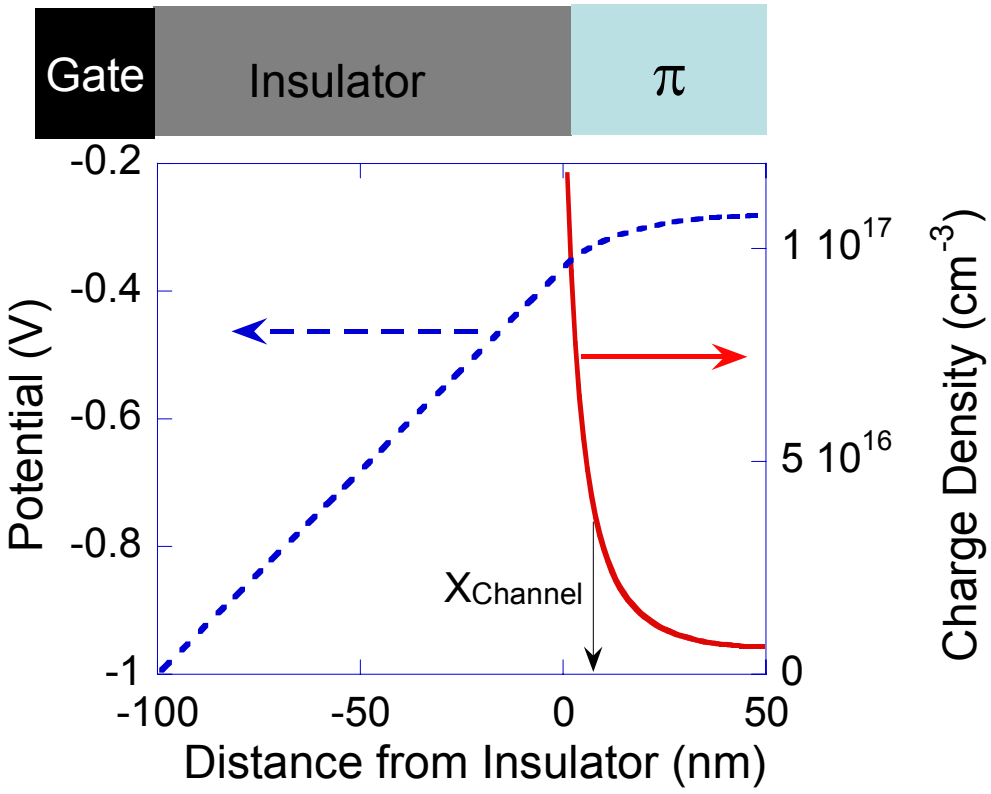

Figure 14. Simulated charge density (2D simulation) and potential at the middle of the channel for p-channel transistor and a bias of $V_{DS}=(V_{GS}-V_T)=-1$. $X_{Channel}$ denotes the effective channel depth (~7nm here).

In the present text we try instead to examine the validity of our assumption and give the reader a feeling for the associated effect on the device performance. To derive and

expression for the charge profile perpendicular to the insulator we start with the basic current continuity and Poisson equations:

$$J_h = qp\mu_h \cdot E - q\frac{\partial}{\partial x}\left(D_h p\right) = qp\mu_h \cdot E - qD_h \frac{\partial}{\partial x} p - qp\frac{\partial}{\partial x} D_h$$

(25)

$$\varepsilon_\pi \varepsilon_0 \frac{\partial E}{\partial x} = p \cdot q$$

At steady-state there is no current flow in the x direction and if we assume $D_h \frac{\partial}{\partial x} p >> p \frac{\partial}{\partial x} D_h$ we arrive at:

(26) $J_h = qp\mu_h \cdot E - qD_h \frac{\partial p}{\partial x} = 0$

and the boundary conditions for the electric field are:

(27) $E\big|_{x=0} = \frac{\varepsilon_{ins}}{\varepsilon_\pi} E_{ins} \approx \frac{\varepsilon_{ins}}{\varepsilon_\pi} \cdot \frac{\left(V_G - V_T\right) - V(y)}{d_{ins}}; E\big|_{x=d_\pi} = 0$

using (26) and the Poisson equation we can derive:

(28) $E\frac{\partial E}{\partial x} = \frac{D_h}{\mu_h}\frac{\partial^2 E}{\partial x^2}$

or

(29) $\frac{1}{2}\frac{\partial}{\partial x}E^2 = \frac{D_h}{\mu_h}\frac{\partial}{\partial x}\frac{\partial E}{\partial x}$

Integrating over x once (assuming D/μ to be a slowly varying function of x):

(30) $\frac{\mu_h}{2D_h}E^2 + C = \frac{\partial E}{\partial x}$

where C is a constant to be determined by the boundary conditions. Integrating between point x to the air interface (d_π) we arrive at:

(31) $\int_x^{d_\pi} \partial x' = \int_E^0 \frac{\partial E'}{\frac{\mu_h}{2D_h}E'^2 + C}$

and if D/μ is approximately constant across the layer:

(32) $E = \sqrt{\frac{2CD_h}{\mu_h}} \tan\left[\sqrt{\frac{C\mu_h}{2D_h}}\left(x - L\right)\right]$

This electric field creates "band" bending across the π-conjugated layer that is directly derived from the existence of charge at the channel. The bending across the entire layer is:

$$(33)\quad \Delta V_{channel} = -\int_0^L E dx = -\sqrt{\frac{2CD_h}{\mu_h}}\int_0^L \tan\left[\sqrt{\frac{C\mu_h}{2D_h}}\left(x-L\right)\right]dx = -\frac{2D_h}{\mu_h}\log\left(\cos\left[\sqrt{\frac{C\mu_h}{2D_h}}L\right]\right)$$

And the charge density across the π-conjugated layer:

$$(34)\quad \boxed{p = \frac{\varepsilon_\pi\varepsilon_0}{q}\frac{\partial E}{\partial x} = \frac{C\varepsilon_\pi\varepsilon_0}{q}\left(\tan\left[\sqrt{\frac{C\mu_h}{2D_h}}\left(x-L\right)\right]^2+1\right)}$$

and C is to be determined by:

$$(35)\quad \frac{\varepsilon_{ins}}{\varepsilon_\pi}E_{ins} = E\big|_{x=0} = \sqrt{\frac{2CD_h}{\mu_h}}\tan\left[\sqrt{\frac{C\mu_h}{2D_h}}\left(0-L\right)\right]$$

To illustrate the use of equations (32) to (35) we calculated the charge density profile for two different electric fields at the insulator (E_0). The first one was chosen to be close to the conditions used for Figure 14 and the second for a higher applied voltage. We first use equation (35) to find the integration constant C (Table 1) and then use equation (34) to calculate the charge density profile (T=300k).

Table 1. The parameters used for Figure 15.

E_{ins} [v/cm]	d_π [cm]	C	$\Delta V_{channel}$ [V]
$5\cdot10^4$	$50\cdot10^{-7}$	3.5457e+009	0.069
$3\cdot10^5$	$50\cdot10^{-7}$	4.7943e+009	0.153

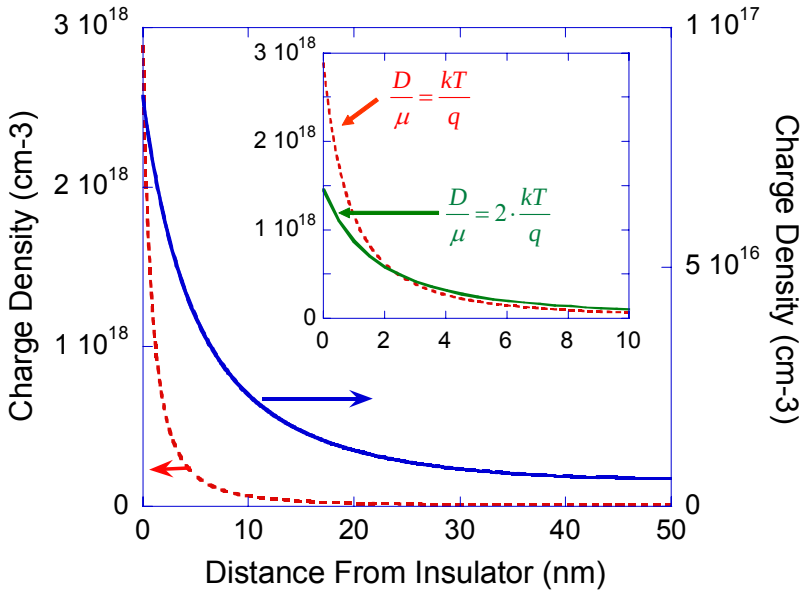

Figure 15. Calculated charge density profile for two electric fields at the insulator (different V_{GS}). The right axis is for $E_0=5\cdot10^4 vcm^{-1}$ and the left axis for $E_0=3\cdot10^5 vcm^{-1}$ ($\varepsilon_\pi=3$). The inset shows the effect of D/μ being a (slowly-varying) function of the charge density ($E_0=5\cdot10^4 vcm^{-1}$). The full line in the inset was calculated using D/μ=2·kT/q (see [21]) and only the first 10nm are shown.

Examining Figure 15 we note that at low voltage drop across the insulator the channel is rather extended and the charge density extends a considerable way into the π-conjugated layer. The functional form of the density distribution tells us that for a thinner π-conjugated layer the effect will be more pronounced. We also note that at higher applied bias the channel becomes more confined as most of the added charge accumulates near the insulator interface. Finally, the inset shows the effect of the enhanced Einstein-relation as discussed in [22], and demonstrates that for higher values of D/μ the charge is more spread across the polymer.

To make the picture complete we mention that it has been shown that organic amorphous (disordered) semiconductors are degenerate at all practical densities[21] and hence $\frac{D}{\mu}=\eta\frac{kT}{q}$ with η being a function of the charge density[21, 22]. For example, using the calculation shown in the inset to Figure 15 (η=2) $\Delta V_{channel}\cong 0.25eV$. Also, a change in the value of the band bending ($\Delta V_{channel}$) is an indication that the chemical potential

(quasi Fermi level, E_F) in the π-conjugated layer is also shifting thus modifying the effective threshold voltage.

Next we move to evaluate a simple expression also for the effective channel depth. If we define $X_{Channel}$ as the point where p drop to 1/e of its value then

$$(36)\quad e^1 = \frac{p_{x_1}}{p_{x_2}} = \exp(-\frac{\mu_{x_1}}{D_{x_1}}\Delta\phi_{12}) \rightarrow \Delta\phi_{12} = -\frac{D_{x_1}}{\mu_{x_1}}$$

If we assume that within the channel depth the electric field has not decayed significantly from its value at the insulator:

$$(37)\quad \frac{\varepsilon_{ins}}{\varepsilon_\pi} E_{ins} X_{Channel} = \frac{D}{\mu}$$

and

$$(38)\quad \boxed{X_{Channel} \approx \frac{d_{ins}}{V_G - V(y)} \frac{\varepsilon_\pi}{\varepsilon_{ins}} \frac{kT}{q} \eta}$$

Using common parameters as $d_{ins} = 100e-7cm; V_{GS} - V_T = 1V; V_{DS} = 1V$ we find that near the source $\left(V_G - V(y) = V_{GS}\right)$ $X_{Channel}$=2.6nm×η and at the centre of the channel $\left(V_G - V(y) - V_T \cong 0.5V\right)$ $X_{Channel}$=5.2nm×η. Note that the approximate expression of equation (37) is in good agreement with the numerical simulation results shown in Figure 14. Namely, in organic transistor where the molecular distance is about 0.5nm the channel will extend over several monolayers, especially at low gate bias. We mention that a more precise expression for $X_{Channel}$ can be derived directly from equation (34) .

6.2 Switch on (transient dynamics)

The use of FETs is largely as a switching element in a circuit the speed of which is determined by the time it takes to switch the transistor on (and off). Therefore it is essential that we have some understanding of the mechanism by which the transistor channel is built as a function of time[23, 24]. We also take this opportunity to look more into the operation of the top contact CIπ-FET structure (see Figure 2). Figure 16 shows the charge density and potential distribution at about 100ns after the gate voltage has

been switched from V_G=0 to V_G=-5V while keeping the source and drain voltage constant at V_S=0 and V_D=-3V, respectively.

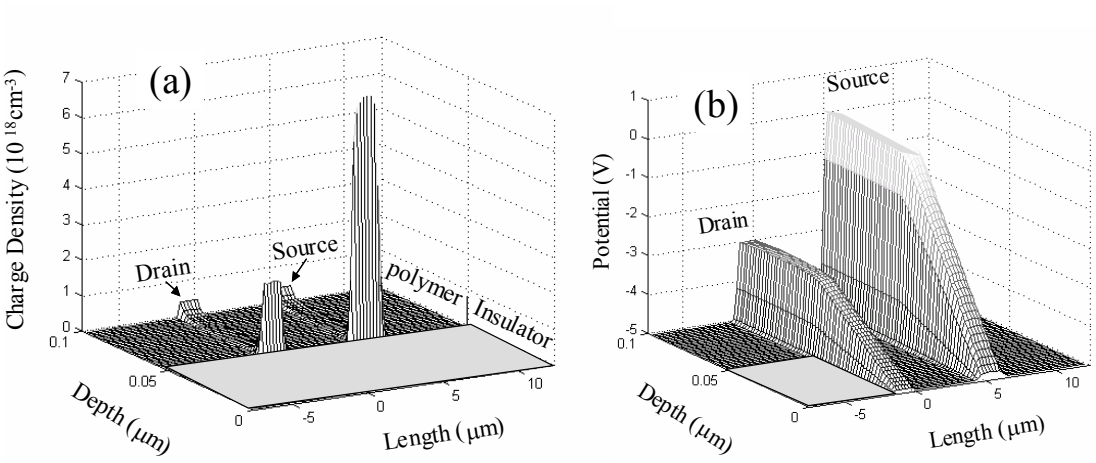

Figure 16. Charge density (a) and potential (b) distribution for a top contact CIπ-FET shortly after switching the gate voltage from 0 to -5V (V_{DS}=-3V).

We note that at first the source and drain are isolated from each other (as the channel that will connect them has not been formed yet). At this short time we see mainly the capacitive nature of the FET structure that was discussed in section 2.1. Namely, the region under the drain and source contacts is charged and the voltage applied to the source and drain is projected onto the insulator interface. This situation is schematically illustrated in Figure 17.

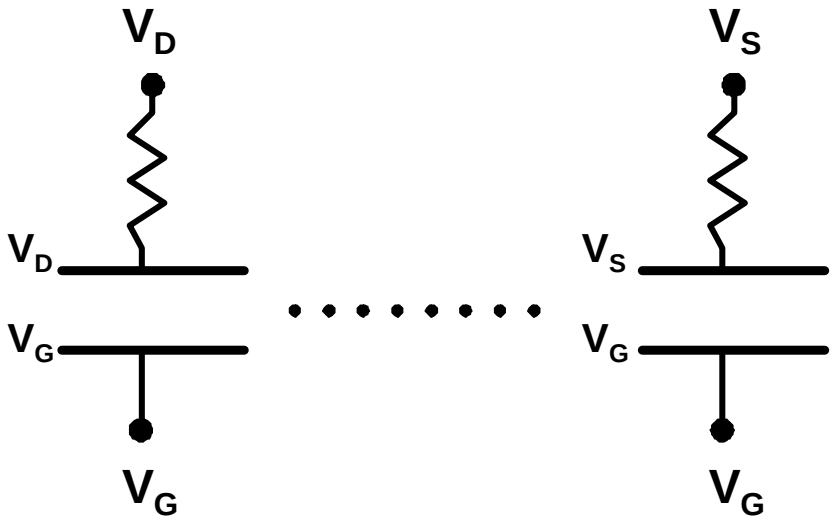

Figure 17. Equivalent circuit description of the FET immediately after switching the gate voltage.

After the source and drain have been projected onto the insulator interface the channel will start to form through the charged regions underneath the contacts. A naïve estimate of the time it would take to build the channel would be to consider the time it would take for a charge to drift the channel length under the applied source drain bias:

$$\Delta t = \frac{L}{\mu E} = \frac{L^2}{\mu V_{DS}} = \frac{\left(5\cdot 10^{-4}\right)^2}{5\cdot 10^{-3}\cdot 3} = 16.66\mu s \quad (39)$$

However, examining Figure 16b we note that at this initial stage the voltage actually drops across a much shorter distance and only across the part of the channel that has been filled (see also equation (5)). In Figure 18 we plot the simulated charge build up at the channel, which is similar[vi] in shape to the potential across it ($P \approx C_{ins} V$). We note that the channel is built within less then 5μs being less then a third of the naïve value of 16.66μs calculated above. The relation between the charge density (P) and the potential (V) has also been used in a time dependent Kelvin-probe measurement to experimentally monitor the channel build-up[24].

[vi] The deviation is related to the potential drop across the channel itself as described in equation (33)

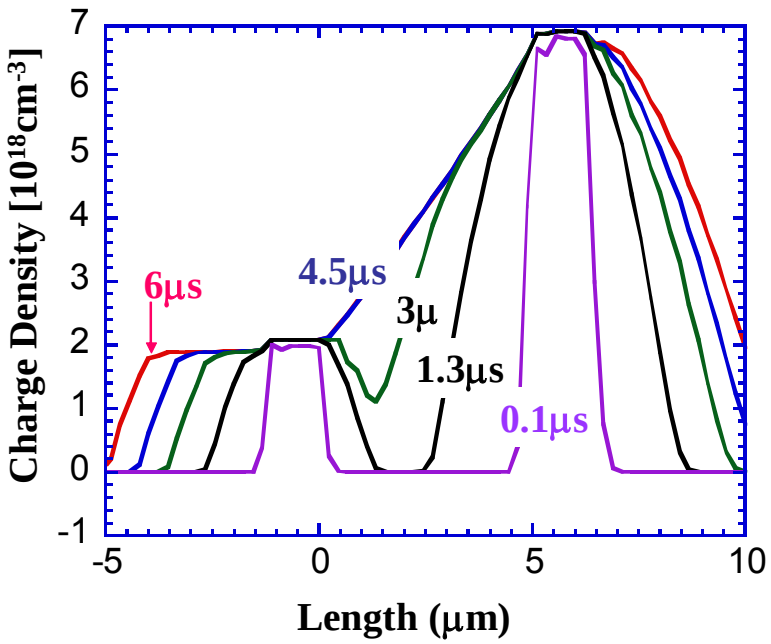

Figure 18. Charge density distribution at the channel as a function of time ($\mu=5\cdot10^{-3}cm^2v^{-1}s^{-1}$) after switch on.

As $P\approx C_{ins}V$ we also note that the drain-source bias drops across the entire channel length only after the entire channel has been formed. Namely, the equivalent circuit describing the channel build up is as shown in Figure 19.

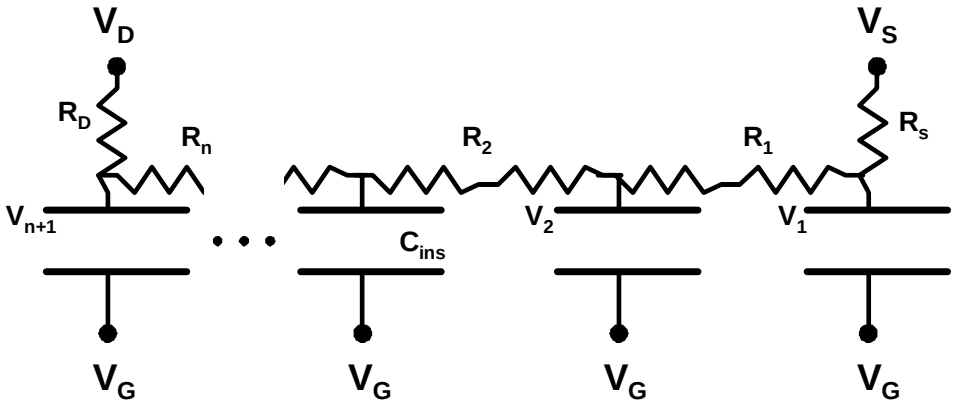

Figure 19. The equivalent distributed circuit describing the channel build up.

In Figure 19 R_S and R_D are the contact resistance which would be negligible in a well behaved FET. R_i are the serial resistance associated with the current that flows through, and fill up, the channel. The resistance, R_i, is derived from the conductivity as:

(40) $R_i = \frac{\Delta L}{A}\frac{1}{q\mu p} = \frac{\Delta L}{d_\pi * W}\frac{1}{q\mu p}$

where ΔL is the distance separating two elements. The charge density p is determined by the voltage (V_i-V_G) that drops across the capacitors next to R_i. Taking VG as the reference potential (V_G=0):

$$R_i = \frac{\Delta L}{d_\pi * W}\frac{1}{q\mu\frac{C_{ins}\frac{|V_i + V_{i+1}|}{2q}\Delta L * W}{d_\pi * \Delta L * W}} = \frac{\Delta L}{W}\frac{1}{\mu C_{ins}\frac{|V_i + V_{i+1}|}{2}}$$

To solve the circuit in Figure 19 we require defining the boundary conditions:

$$\begin{cases} V_1 = V_S - V_G; V_{n+1} = V_D - V_G; \\ for\ i \neq 1, n+1\ V_i\big|_{t=0} = 0 \end{cases}$$

and for the dynamics of the system we rely of the capacitor characteristics $\left(I_i = c\frac{dV_i}{dt}\right)$

and on kirchof law $I_i = I_{R_{i-1}} - I_{R_i}$:

(41) $$\frac{dV_i}{dt} = \frac{1}{C_{ins}\cdot W\cdot \Delta L}\left(\frac{V_{i-1} - V_i}{R_{i-1}} - \frac{V_i - V_{i+1}}{R_i}\right)$$

and if μ is field and density independent and V_i are all positive we arrive at an expression similar to the continuous form[24]:

(42) $$\frac{dV_i}{dt} = \frac{\mu}{2\Delta L^2}\left(V_{i-1}^2 - 2V_i^2 + V_{i+1}^2\right)$$

and finally the transient currents are:

(43) $$\begin{cases} I_S(t) = \frac{(V_S - V_G) - (V_2(t) + V_T)}{R_1} \\ I_D(t) = \frac{(V_D - V_G) - (V_n(t) + V_T)}{R_n} \end{cases}$$

The above equations suggest that the transistor switch on characteristics are rather universal and only depend on the channel length and the insulator capacitance. However, there is a hidden dependence which may make the transient curve material dependent. Since the mobility may be charge density dependent [25-28] and this dependence varies

with the morphology of the π-conjugated layer the functional form of this transient curve is no longer necessarily universal in shape.

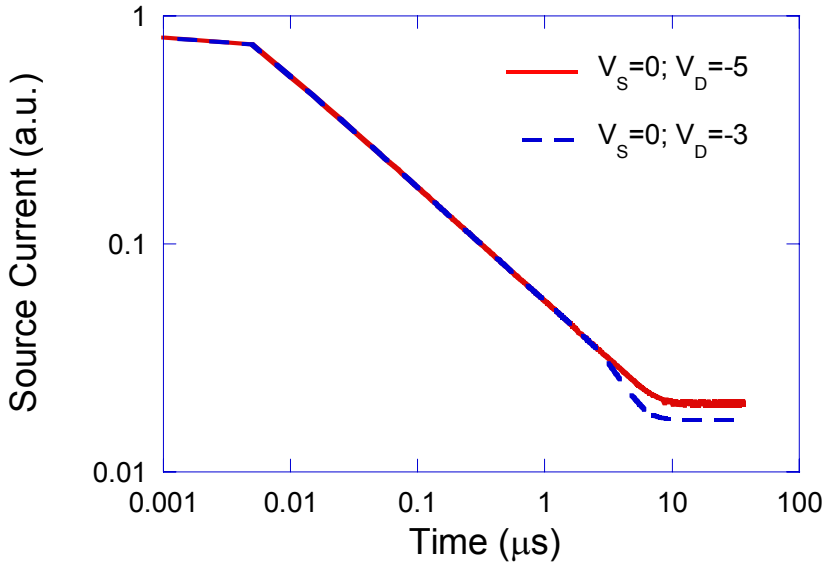

Figure 20. Calculated (Eq.(43)) current transient for a gate voltage step between 0 and -5V. The solid line is calculated for V_{DS}=-5V and the dashed line for V_{DS}=-3V.

To illustrate the use of equations (40) to (43) we have calculated the current transient measured at the source using parameters similar to those used in the 2D numerical simulation that resulted in Figure 18. The solid line is calculated for V_{GS}=V_{DS}=-5V and the dashed line for V_{DS}=-3V. We note that the two curves are identical but for the last microseconds. This is expected since at early times the drain voltage has no effect on the charge density near the source contact (see Figure 18). Examining Figure 18 we note that the charge distribution near the drain affects the source only at about t=3μs, which is in very good agreement with the point at which the two curves in Figure 20 start to deviate. Namely, equations (40) to (43) are a reasonably good approximation for the physical picture studied here.

Acknowledgment

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REFERENCES

[1] **J. H. Burroughes, C. A. Jones, and R. H. Friend, "Polymer Diodes and Transistors: New Semiconductor Device Physics," *Nature*, vol. 335, pp. 137-141, 1988.**

[2] **A. R. Brown, A. Pomp, C. M. Hart, and D. M. Deleeuw, "Logic gates made from polymer transistors and their use in ring oscillators," *Science*, vol. 270, pp. 972-974, 1995.**

[3] **C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, and D. M. de Leeuw, "Low-cost all-polymer integrated circuits," *Appl. Phys. Lett.*, vol. 73, pp. 108-110, 1998.**

[4] **B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. Laduca, R. Sarpeshkar, H. E. Katz, and W. Li, "Large-scale complementary integrated circuits based on organic transistors," *Nature*, vol. 403, pp. 521-523, 2000.**

[5] **S. R. Forrest, "Active optoelectronics using thin-film organic semiconductors," *IEEE J. Sel. Top. Quantum Electron.*, vol. 6, pp. 1072-1083, 2000.**

[6] **G. Horowitz, F. Deloffre, F. Garnier, R. Hajlaoui, M. Hmyene, and A. Yassar, "All-organic field-effect transistors made of pi-conjugated oligomers and polymeric insulators," *Synth. Met.*, vol. 54, pp. 435-445, 1993.**

[7] **W. Fix, A. Ullmann, J. Ficker, and W. Clemens, "Fast polymer integrated circuits," *Appl. Phys. Lett.*, vol. 81, pp. 1735-1737, 2002.**

[8] **F. Garnier, R. Hajlaoui, A. Yassar, and P. Srivastava, "ALL-POLYMER FIELD-EFFECT TRANSISTOR REALIZED BY PRINTING TECHNIQUES," *Science*, vol. 265, pp. 1684-1686, 1994.**

[9] **M. G. Kane, J. Campi, M. S. Hammond, F. P. Cuomo, B. Greening, C. D. Sheraw, J. A. Nichols, D. J. Gundlach, J. R. Huang, C. C. Kuo, L. Jia, H. Klauk, and T. N. Jackson, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Lett.*, vol. 21, pp. 534-536, 2000.**

[10] **T. Granlund, T. Nyberg, L. S. Roman, M. Svensson, and O. Inganas, "Patterning of polymer light-emitting diodes with soft lithography," *Adv. Mater.*, vol. 12, pp. 269-273, 2000.**

[11] **D. Pede, G. Serra, and D. Derossi, "Microfabrication of conducting polymer devices by ink-jet stereolithography," *Mater. Sci. & Engineering C - Biomimetic Mater. Sensors & Systems*, vol. 5, pp. 289-291, 1998.**

[12] **J. A. Rogers, Z. Bao, M. Meier, A. Dodabalapur, O. J. A. Schueller, and G. M. Whitesides, "Printing, molding, and near-field photolithographic methods for patterning organic lasers, smart pixels and simple circuits," *Synth. Met.*, vol. 115, pp. 5-11, 2000.**

[13] **H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated Optoelectronic Devices based on Conjugated Polymers," *Science*, vol. 280, pp. 1741-1743, 1998.**

[14] **A. Dodabalapur, Z. Bao, A. Makhija, J. Laquindanum, V. Raju, Y. Feng, H. Katz, and J. Rogers, "Organic smart pixels," *Appl. Phys. Lett*, vol. 73, pp. 142-144, 1998.**

[15] **H. E. A. Huitema, G. H. Gelinck, J. B. P. H. Van der putten, K. E. Kuijk, K. M. Hart, E. Cantatore, and D. M. De leeuw, "Active-matrix displays driven by solution processed polymeric transistors," *Adv. Mater.*, vol. 14, pp. 1201-+, 2002.**

[16] **C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, "Organic thin-film**

transistor-driven polymer-dispersed liquid crystal displays on flexible polymeric substrates," *Appl. Phys. Lett.*, vol. 80, pp. 1088-1090, 2002.

[17] Y. Roichman and N. Tessler, "Structures of polymer field-effect transistor: Experimental and numerical analyses," *Applied Physics Letters*, vol. 80, pp. 151-153, 2002.

[18] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.

[19] A. R. Brown, C. P. Jarrett, D. M. deLeeuw, and M. Matters, "Field-effect transistors made from solution-processed organic semiconductors," *Synthetic Metals*, vol. 88, pp. 37-55, 1997.

[20] E. J. Meijer, C. Detcheverry, P. J. Baesjou, E. van Veenendaal, D. M. de Leeuw, and T. M. Klapwijk, "Dopant density determination in disordered organic field-effect transistors," *Journal of Applied Physics*, vol. 93, pp. 4831-4835, 2003.

[21] Y. Roichman and N. Tessler, "Generalized Einstein relation for disordered semiconductors - Implications for device performance," *Applied Physics Letters*, vol. 80, pp. 1948-1950, 2002.

[22] Y. Roichman, Y. Preezant, and N. Tessler, "Analysis and modeling of organic devices," *physica status solidi (a)*, vol. 201, pp. 1246-1262, 2004.

[23] N. Tessler and Y. Roichman, "Two-dimensional simulation of polymer field-effect transistor," *Applied Physics Letters*, vol. 79, pp. 2987-2989, 2001.

[24] L. Burgi, R. H. Friend, and H. Sirringhaus, "Formation of the accumulation layer in polymer field-effect transistors," *Applied Physics Letters*, vol. 82, pp. 1482-1484, 2003.

[25] M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Physical Review B*, vol. 57, pp. 12964-12967, 1998.

[26] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors," *J. Appl. Phys.*, vol. 87, pp. 4456-4463, 2000.

[27] Y. Roichman and N. Tessler, "Charge transport in conjugated polymers - the influence of charge concentration," *Synthetic Metals*, vol. 135-136, pp. 443-444, 2003.

[28] S. Shaked, S. Tal, R. Roichman, A. Razin, S. Xiao, Y. Eichen, and N. Tessler, "Charge Density and Film Morphology dependence of Charge Mobility in Polymer Field Effect Transistors," *Adv. Mat.*, to be published.