Order is Power: Selective Packet Interleaving for Energy Efficient Networks-on-Chip

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The power wall

- Power density continues to get worse

We need to reduce power consumption.

* Source: Gelsinger, ISSCC 2001
Interconnects consume up to 60% of total power.

*Source: ITRS 2001 Edition*
Our goal is to reduce the power consumption on NoC links.
Opportunity: reduce the number of bit transitions on the link

- Dynamic power consumption origins form bit transitions
  - Circuit nodes are being charged

Goal: reduce the number of bit transitions.
Observation

- There are multiple virtual channels in the router

There is flexibility in interleaving.
Observation: example

Two packets in two virtual channels are transmitted

- A 4-bit flit is sent on the link

Can we reduce the number of bit transitions?
Selective Packet Interleaving (SPI)

- Transmit the flit that entails minimum bit transitions

![Diagram](image)

If $D(VC_1, \text{Link}) \leq D(VC_2, \text{Link})$ then transmit the flit from VC1
If $D(VC_2, \text{Link}) < D(VC_1, \text{Link})$ then transmit the flit from VC2

SPI multiplexes flits to the router's output link so as to minimize the number of bit transitions from the previously transmitted flit.
SPI scalability

If there are more VCs, there is a higher probability for lower bit transitions

SPI is scalable with the number of VCs.
SPI overhead

Changes to NoC’s router: add SPI modules.

SPI – Select the minimum Hamming distance

\[ \arg \min_{1 \leq i \leq m} d_H(f_{\text{LINK}}, f_i) \]
Analysis results

For 8b links, SPI outperforms *Bus Invert* (BI) starting from two VCs. For 16b and 32b links, SPI outperforms BI starting from three VCs.

SPI and BI improvement over uncoded

SPI+BI improvement over uncoded
As the ratio #VCs/(link width) increases, the percentage of improvement over uncoded transmissions increases, and the gap between SPI and SPI+BI shrinks.
Benchmark simulations

The percentage of improvement is similar for all benchmarks. With two VCs and 16b links, the improvements are 10% to 13%. With eight VCs and 8b links, the improvements are 45% - 55%.
SPI was implemented in VLSI design tools to test for power consumption.

For 8b width links and four VCs, we observe more than 25% power reduction. For 16b width links and four VCs, we observe 15% power reduction. For 32b width links and four VCs, the reduction is about 10%.
Selective packet interleaving statistically reduces the number of bit transitions.

Selective packet interleaving can reduce the power consumption of the NoC.
   • Less bit transitions

Selective packet interleaving is scalable with the number of VCs.
Thank you for your time.

Questions session.