Low Overhead Error Detection For Networks-on-Chip

Amit Berman and Idit Keidar

Department of Electrical Engineering,
Technion – Israel Institute of Technology

Agenda

- **Reliability in Network-on-Chip**
- **"*Parity Routing*" (PaR)**
- **The advantages of "*Parity Routing*"**
  - **Network Traffic**
  - **VLSI performance, area and power**
- **Conclusions**

Introduction

- **Modern VLSI systems introduce deep sub-micron noises**
  - **Crosstalk, Radiation, EMI, Process variations…**
  - **As device shrinks, new error sources emerge**

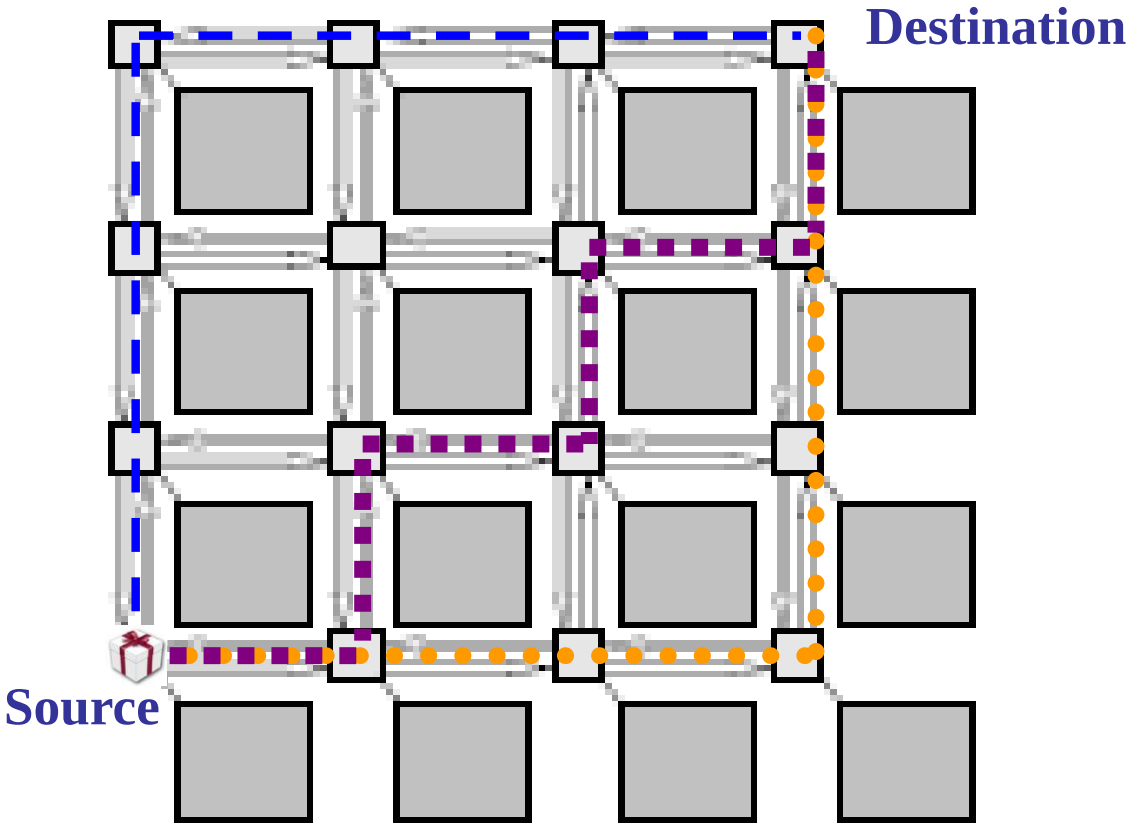
- **Error protection coding modules are used to reduce error probability**
  - **Add redundant traffic over VLSI links / NoC routing paths**

Our goal is to reduce the overhead resulting from error coding modules

Observation

➢There are several routing paths between source and destination

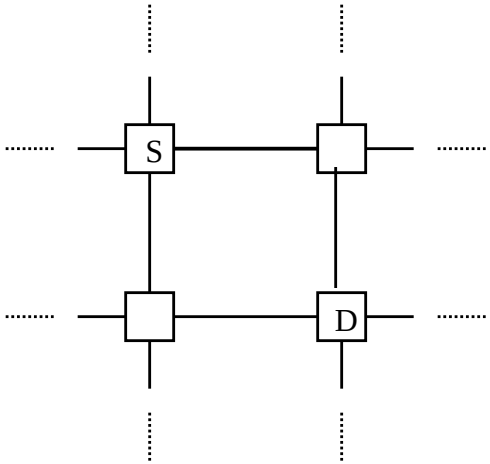
- Assuming shortest-path routing



Observation: Example

➢**XY and YX paths between S and D**

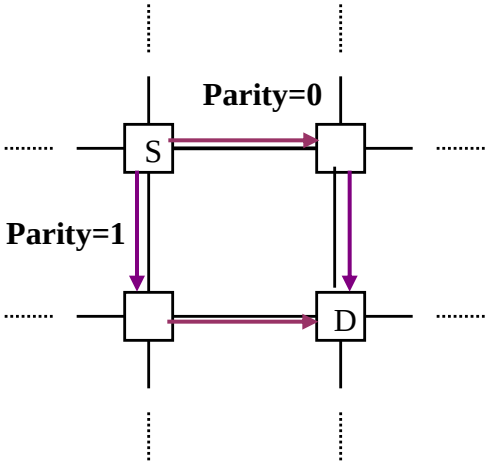
- **A packet consists of N information bits and 1 parity bit is sent from S to D**



Can we save the parity bit's transmission?

Parity Routing (PaR)

➢Route the information according to the parity bits



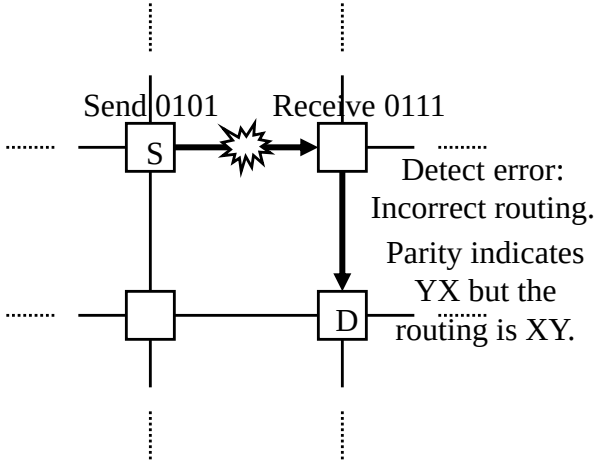
If Parity=0: Route XY
If Parity=1: Route YX

PaR Concept

Route the packet through a chosen path out of all available routing paths according to the parity bits value

PaR Error Detection Concept

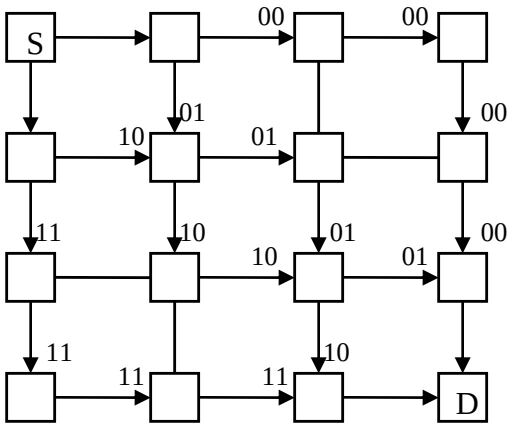
- **Calculate parity bits at the receiving hop and compare to the expected bits of the routing path**



If there is no path diversity between the source and destination nodes, PaR does not reduce the redundant traffic

PaR Concept (2)

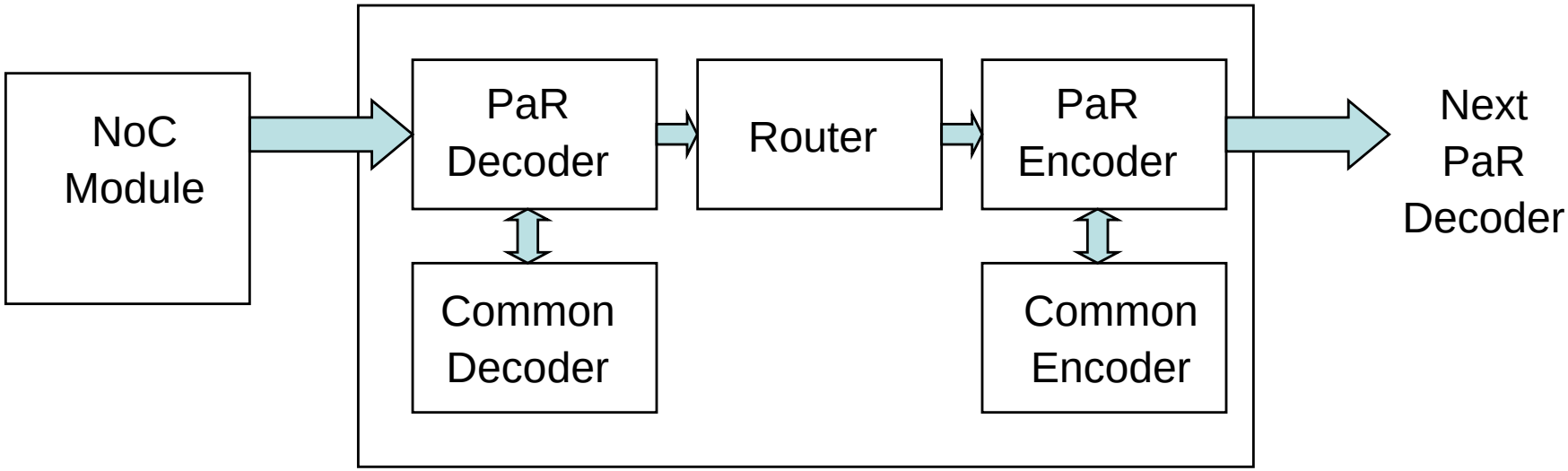
- If there are more paths, we save more bits



PaR is scalable – the savings increase asymptotically to 100% with the size of the NoC.

PaR: Changes To The Current Error Coding Modules

➢PaR works with existing error encoding schemes



➢Changes to NoC's network interfaces:

Add PaR coding modules to NoC routers

Change the control logic for conventional error decoder

Analysis

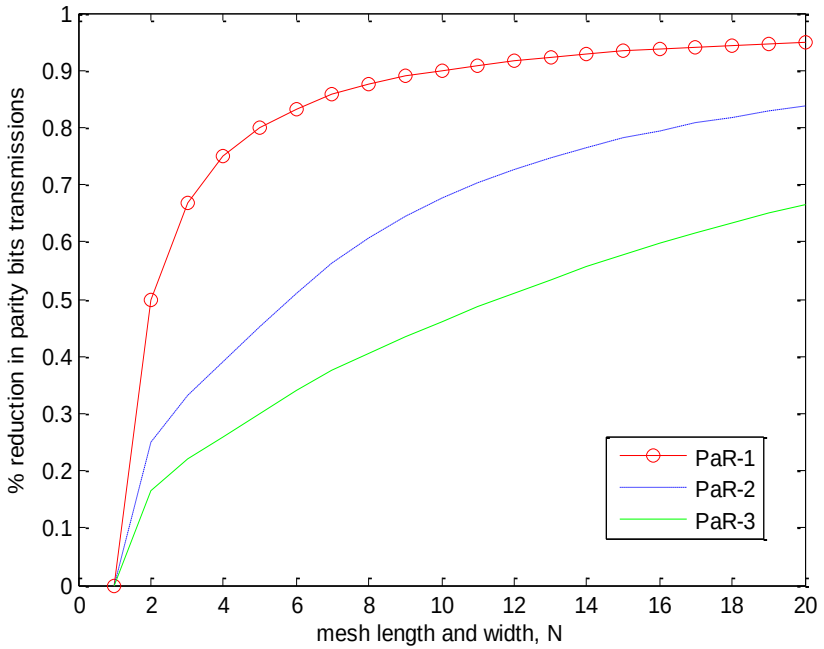
Denote by $CR_1(N,M)$ the percentage of edges on the paths between all the S-D pairs for which the redundant bit is not sent by PaR-1, on an NxM NoC mesh:

$$CR_1(N,N) = 1 - \frac{2N(N-1)}{2N(N-1)+2N(N-1)^2} = \frac{N-1}{N}$$

$$\lim_{N\to\infty} CR_1(N,N) = 1$$

$$\lim_{N\to\infty} CR_1(N,\alpha N) = 1$$

$$CR_r = \frac{2\cdot(r-1)\left(2^{r-1}-1\right)}{d_x(S,D)+d_y(S,D)}$$



Example

For 4x4 NoC mesh and 1 redundant parity bit (PaR-1):

$$CR_1(4,4) = \frac{N-1}{N} = \frac{3}{4}$$

➢**Hence, 75% of the redundant bits transmissions are saved**

For 2 redundant parity bits (PaR-2), where S=(0,0) and D=(2,2)

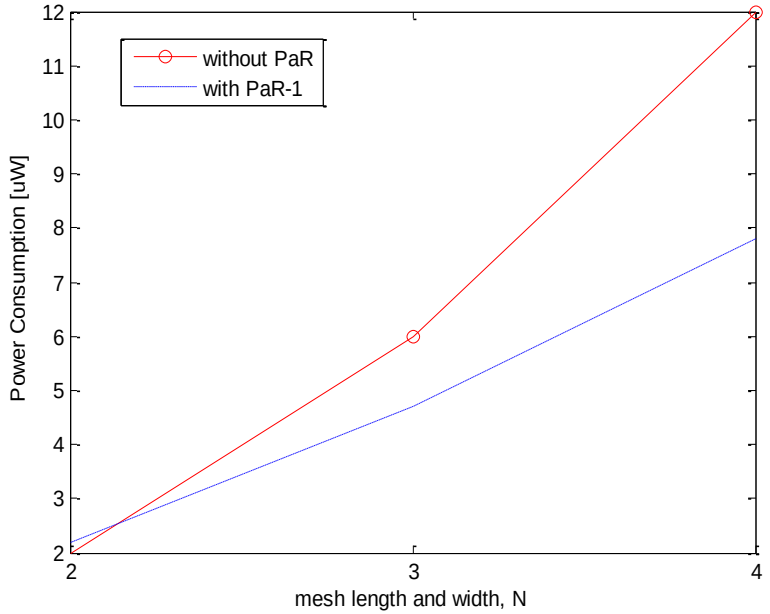
$$CR_2 = \frac{2\cdot(r-1)\left(2^{r-1}-1\right)}{d_x(S,D)+d_y(S,D)} = \frac{1}{2}$$

→ **Saves 50% of redundant bits transmissions between S and D**

*** Taking into account uniform random traffic pattern**

Power Reduction

PaR was implemented on Verilog model and synthesized to test for power consumption



For 2x2 NoC, the encoder and decoder blocks overhead do not compensate for the power reduction achieved by the reduced redundant bits traffic. For 3x3 NoC, savings are over 25%, and for 4x4 NoC, more than 35%.

Summary

- ***Parity Routing*** **statistically reduces redundant bit transmission**
  - **Can be used to reduce wires**
  - **Can be use to increase network's traffic**

- ***Parity Routing*** **can reduce the power consumption of the NoC**
  - **Less bit transmissions, simple error decoding process**

- ***Parity Routing*** **is scaleable, load balanced and reduce the overhead of error detection in NoC**

Questions?