



Technion – Israel Institute of Technology

Electrical Engineering Department – VLSI Lab

Fast Asynchronous Shift Register for Bit-Serial Communication

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ASYNC06

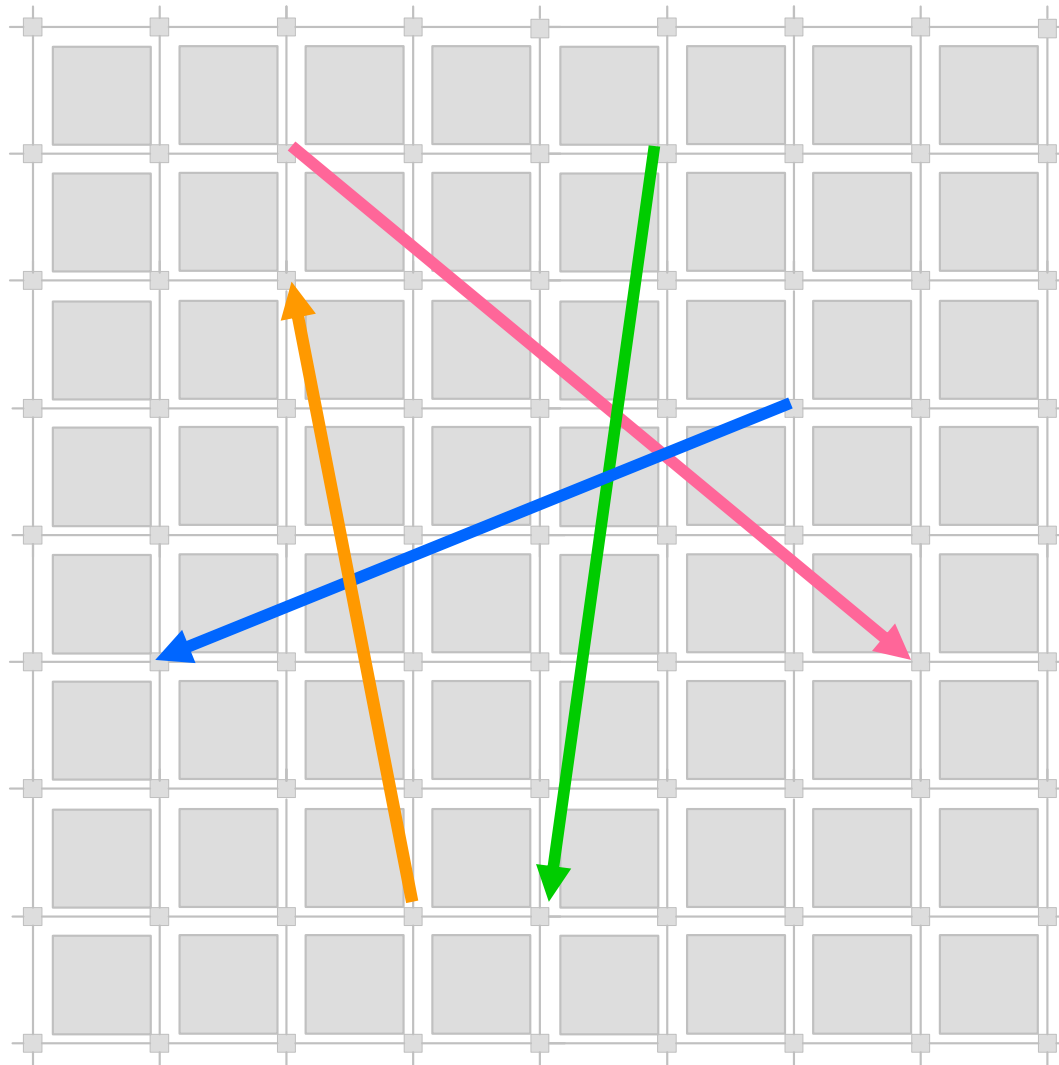


Presentation Outline

- On-Chip Communication Challenges
- Fast Asynchronous Serial Communication
 - Transmitter
 - Channel
 - Receiver
- High Data Rate Asynchronous Shift Register
- Performance
- Conclusions



A Future SoC + NoC Structure



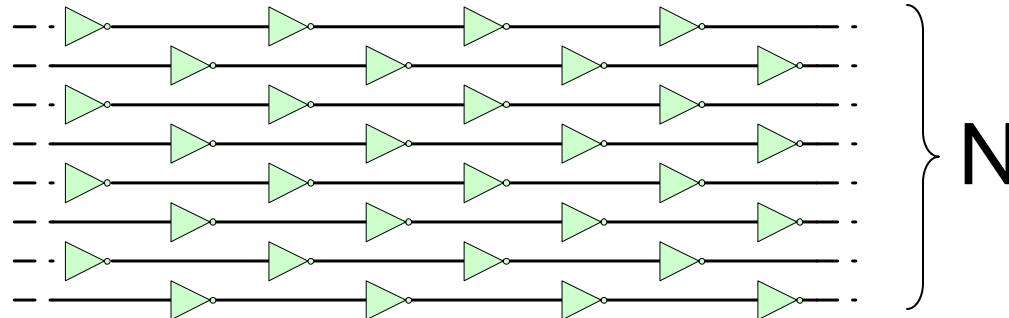


On-Chip Communication Challenges

- Low Power
- High Throughput (bit-per-second)
- Low-Latency Synchronization
- Total Low Latency (fly time from source to sink)
- Low Area (routability)
- High Reliability



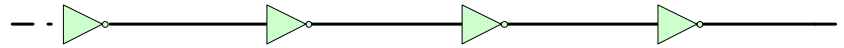
Parallel NoC Links and SoC Buses



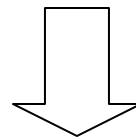
- Constructed of multiple wires and repeaters
- Incur high leakage power (line drivers and repeaters)
- Often have low utilization (leakage again)
- Occupy large chip area (routing difficulty)
- Incur cross-coupling (delay matching & skew problems)
- Present a significant capacitive load



Bit-Serial Interconnect



- Fewer lines, fewer line drivers and fewer repeaters



- Reduced leakage power
- Reduced chip area
- Better routability
- Reduced coupling

BUT

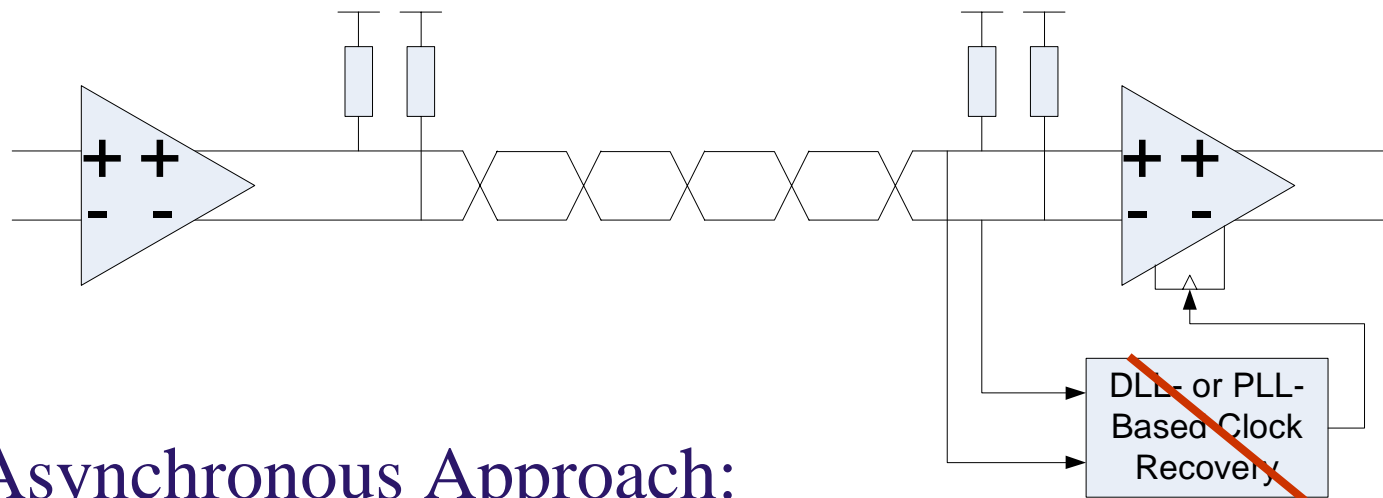
- Should work N times faster!

$$F_{\text{SER}} = N \times F_{\text{PAR}}$$



Fast Serial Interconnect

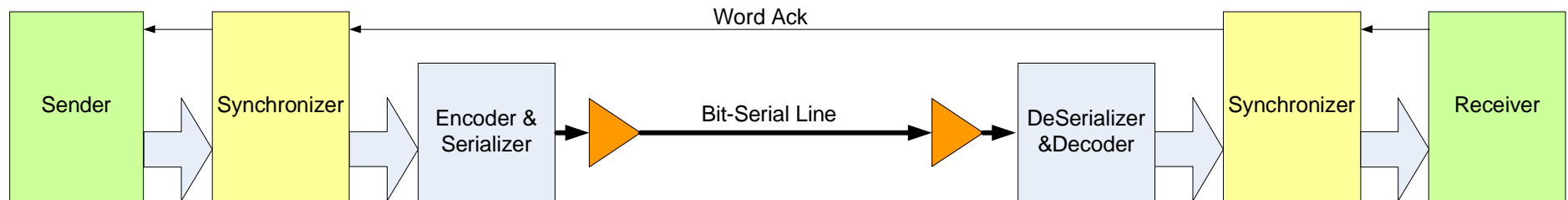
- Synchronous Approach:
 - Source-synchronous, with Clock Data Recovery (CDR)
 - Problem: CDR power and area



- Asynchronous Approach:
 - Normal methods are too slow
 - *We consider a faster one*



Serial Link – Top Structure

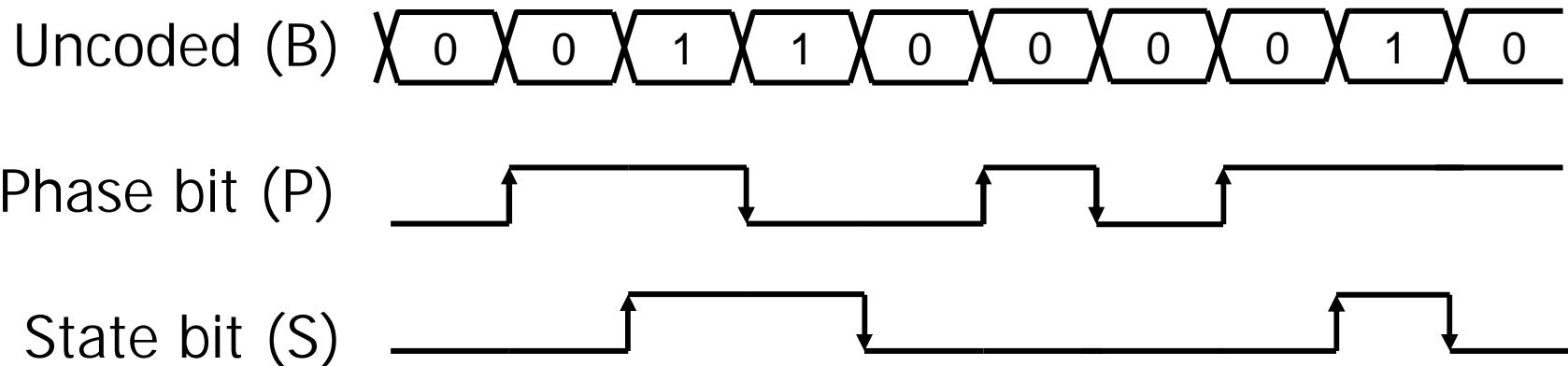


- Transition signaling instead of sampling: two-phase NRZ Level Encoded Dual Rail (LEDR) asynchronous protocol
- Acknowledge per word instead of per bit
- Wave-pipelining over channel
- Differential encoding
- Low-latency synchronizers



Encoding – Two Phase NRZ LEDR

- Two Phase Non-Return-to-Zero Level Encoded Dual Rail
 - “delta” encoding (one transition per bit)

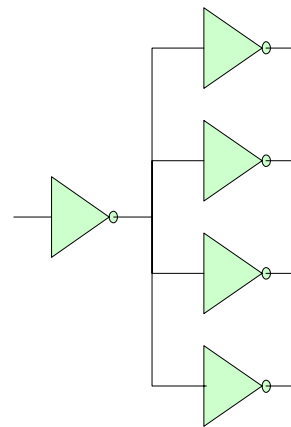




Seeking Highest Speed

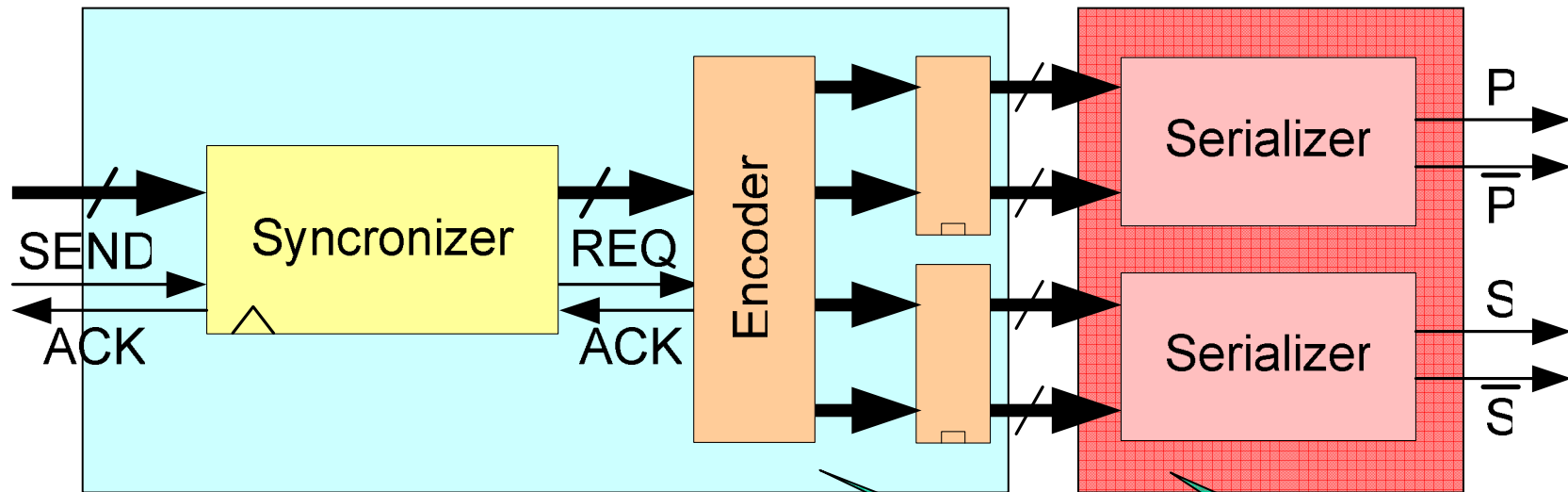
- No “spacers” (NRZ)
- One transition per bit
- Fast signaling
 - Targeted Speed: One gate delay between bits
 - For 65nm technology this results in 67 Gbps

One Gate Delay
=
FO4 INV Delay





Transmitter – Top Architecture



- Main Functions:

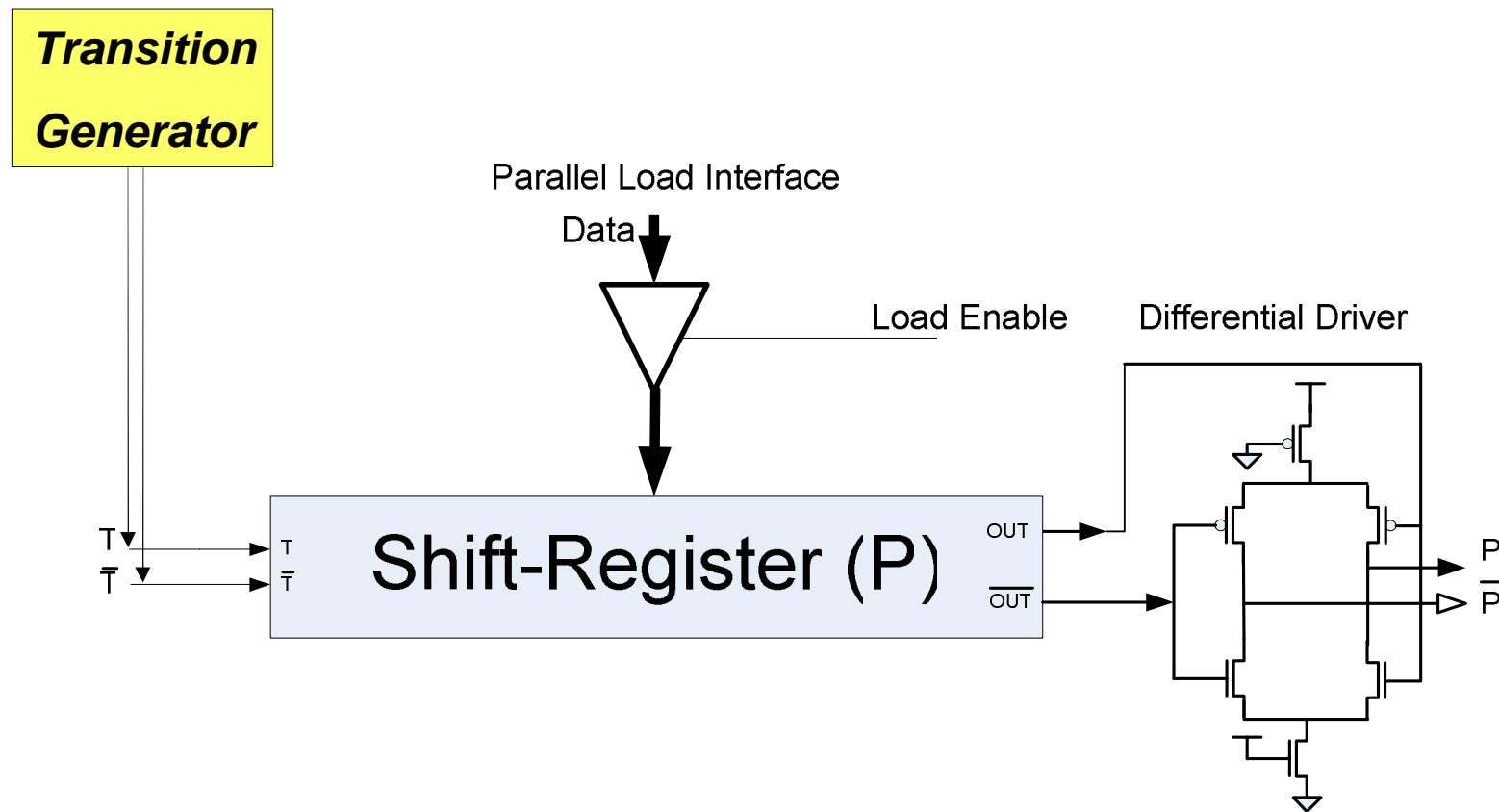
- Synchronizer (Standard, LDL)
- Dual-Rail Two-Phase Encoder (AFSM)
- Serializer (A Novel Solution)
- Differential Encoder (Differential Driver)

**Fast Serial
Operation**

**Slow Parallel
Operation**



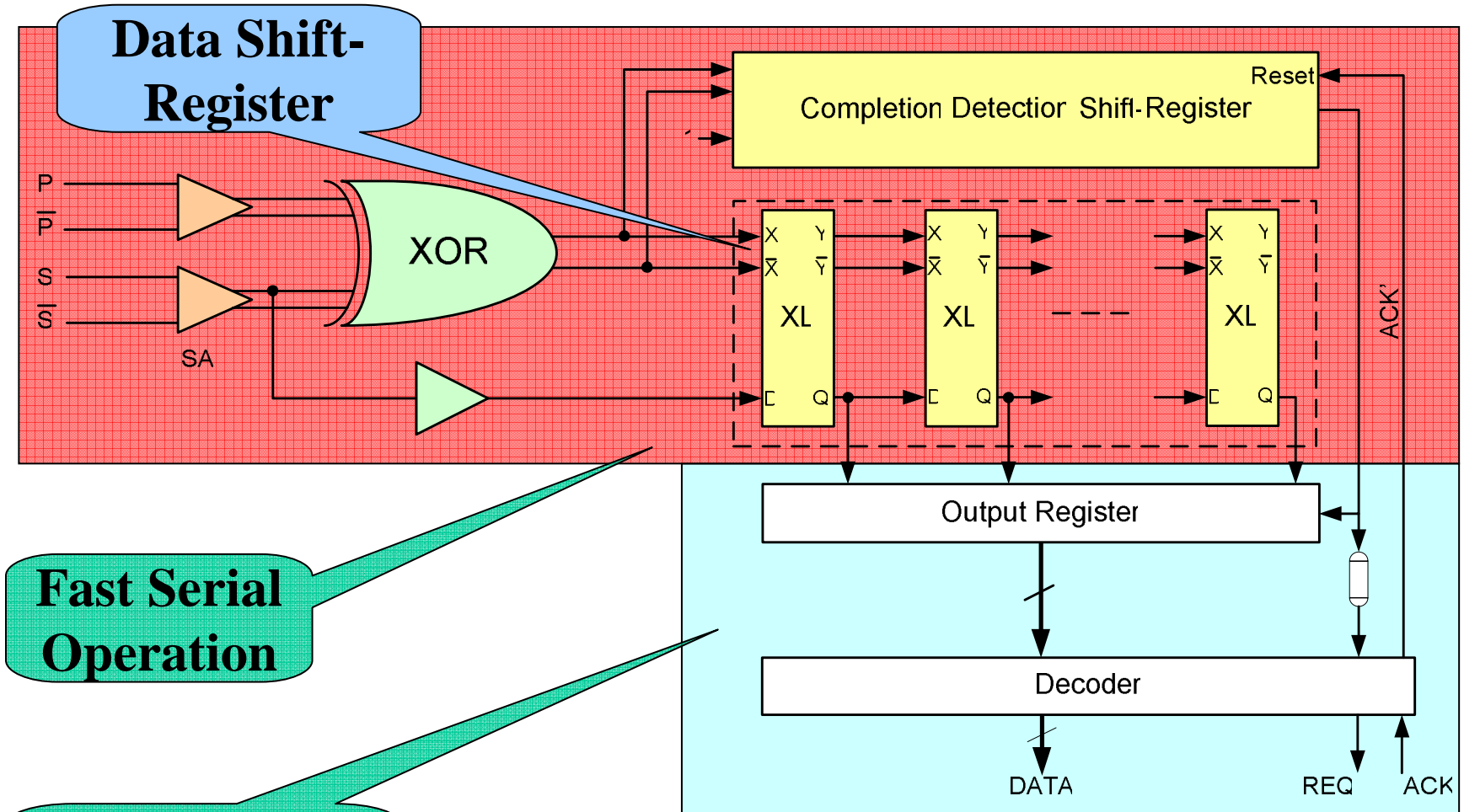
Serializer – Fast SR Approach



- Same circuit drives S , \bar{S} lines

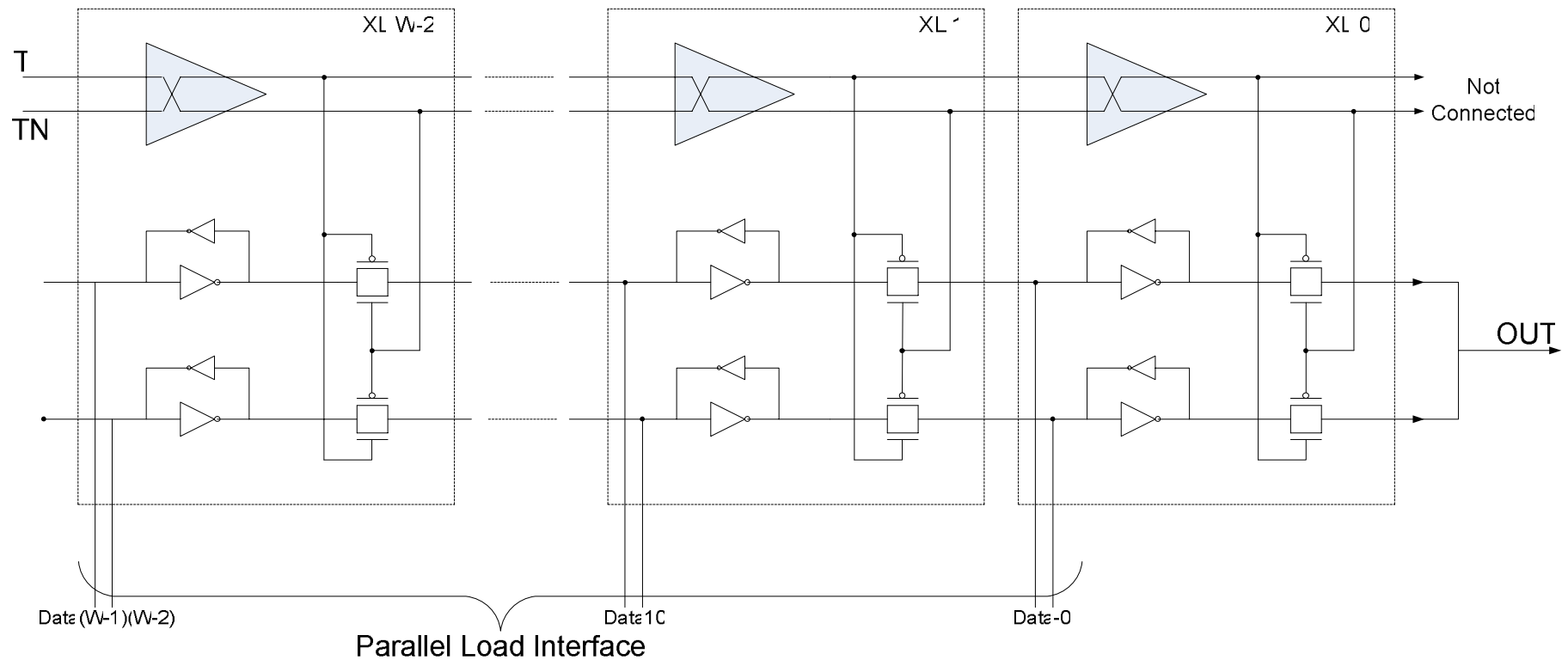


RX – De-Serializer and Decoder



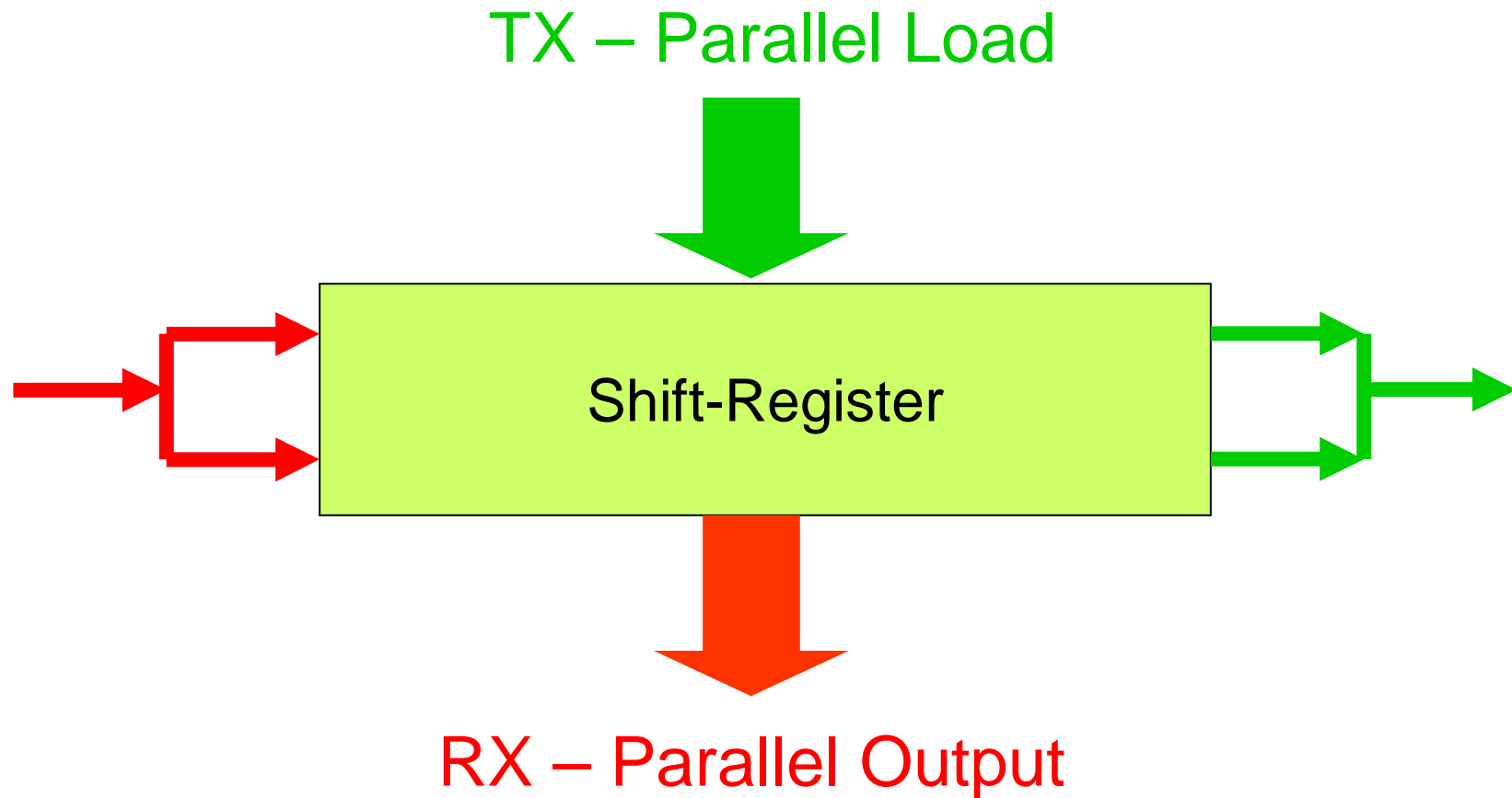


Fast Asynchronous Shift Register



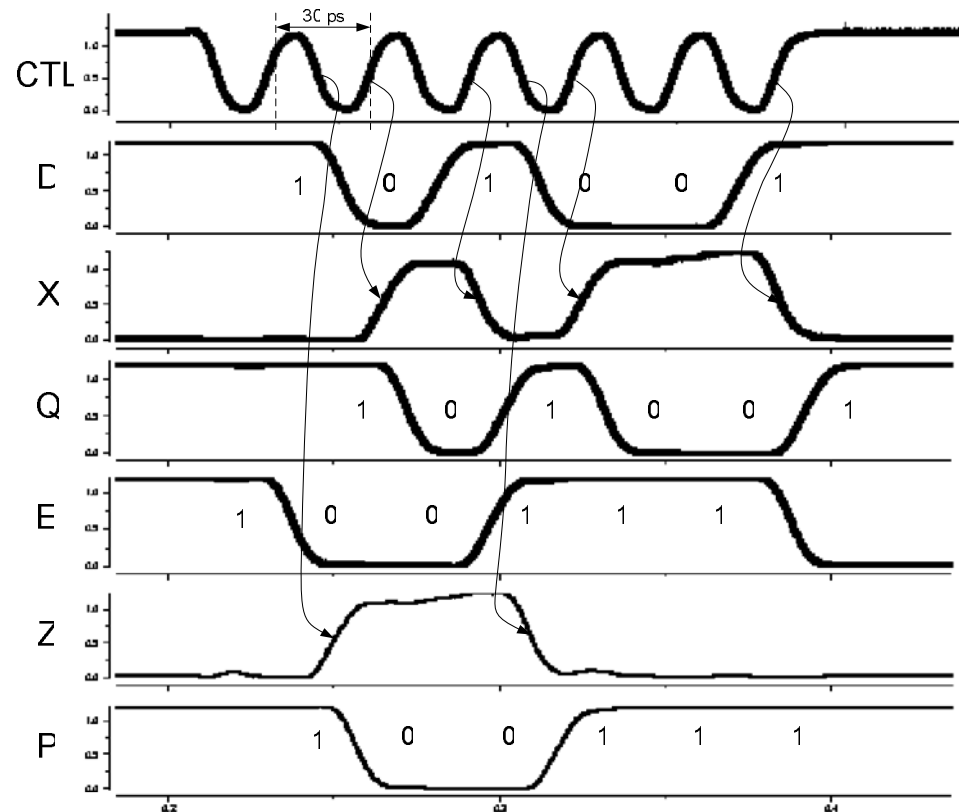
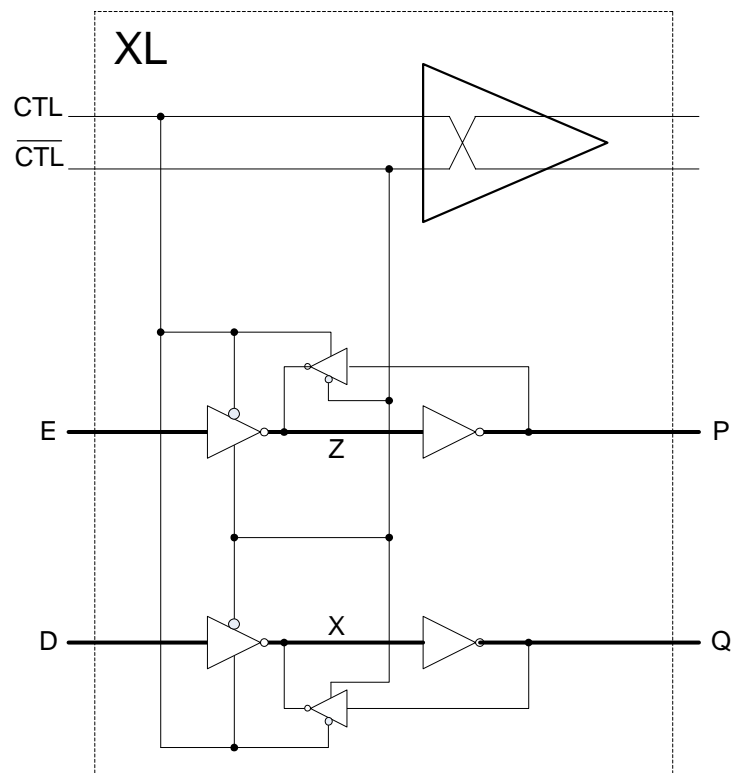


Shift-Register Configurations





Circuitry & Performance



- For typical conditions SR worked down to 14ps data cycle (71Gbps)
- Data is shifted inside sub-pipes twice slower than transition rate



Performance

- SPICE simulation show correct operation at target data cycle of 15ps
- SR is asynchronous – allows non-uniform delay intervals between successive bits



- Verified at 24 PVT corners (0.7-1.35V, -10-110°C)
- Verified up to 10σ in-die variation in L_{EFF} and V_T (Monte-Carlo simulations)



Conclusions

- Novel Asynchronous Communication scheme
 - Wave-pipelining over the channel
 - Word-acknowledgement instead of bit-acknowledgement
 - LEDR encoding and differential signaling
- Fast serializers and de-serializers
 - Based on the fast shift register
- Data cycle of a single FO4 inverter delay
 - 15ps on 65nm process, 67 Gbps
- Robust to in-die variations
 - Thanks to asynchronous design
- The fast SERDES is useful for high-bandwidth long on-chip interconnects, where bit serial communication is preferred thanks to reduced area, easier routing and reduced leakage