

# Data Synchronization Issues in GALS SoCs

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## Abstract

*Locally generated, arbitrated clocks for GALS SoCs [1] face the risk of synchronization failures if clock delays are not accounted for. The problem is analyzed based on clock delays, cycle times, and complexity of the asynchronous port controllers. A number of methods are presented. In some cases, it is sufficient to extract all the delays and verify whether the system is susceptible to metastability. In other cases, when high data bandwidth is not required, asynchronous synchronizers or matched-delay asynchronous ports may be employed. Arbitrated clocks may be traded off for locally delayed input and output ports, facilitating high data rates. The latter circuits have been simulated, to verify their performance.*

## 1. Introduction

As systems on chip (SoC) become larger and faster, it is becoming increasingly difficult to distribute a single synchronous clock to the entire chip [2]. To overcome this problem, a Globally Asynchronous, Locally Synchronous (GALS) architecture has been proposed [3]. The ability to run at different frequencies (and different supply voltages) also contributes to power savings. Other reasons to adopt GALS methodology include the need to interface with multiple external clock domains. The principal challenge of GALS architectures is the need to synchronize data as it crosses different clock domains inside the SoC. Two principal clocking and synchronization methods have been proposed to address this issue. Clock synchronization employs handshake clocks that are stopped based on inputs from other domains [4]. Arbitrated locally generated clocks have been proposed in [1][5][6][7]. According to this methodology, a local ring-oscillator based clock generator in each synchronous “island” incorporates a set of MUTEX arbiters that stop the clock temporarily

when new input data arrive. A stoppable clock technique for GALS pipelines [8], which does not employ MUTEX arbiters, accounts for clock tree delays by means of an expensive delay matching circuit and is based on accurate timing analysis of the clock tree. That solution is suitable only for pipelines and not for general GALS SoCs. In this paper, we analyze the effect that the delays through the clock distribution networks might have on synchronization. We show that such delays, which were unaccounted for in previous publications on general GALS architectures, may lead to failures. We also present a variety of solutions to this problem.

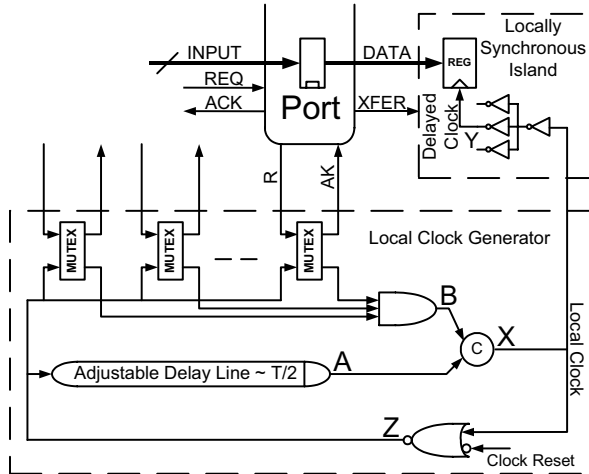
Standard GALS clocking and synchronization is reviewed in Section 2, and their potential for failure is analyzed in Section 3. Proposed solutions are presented in Section 4 and the simulations of some of them are discussed in Section 5.

## 2. Synchronization in locally-clocked GALS SoC

Clocking and input synchronization circuits for locally-clocked SoC proposed in the literature [1][5][6][7] are mostly variations of the circuit in Figure 1. Note the five different components of the clock, namely A, B, X, Y and Z.

A locally generated stoppable clock is employed in each Locally Synchronous Island. Input and output to other islands are controlled by asynchronous handshake via special ports. The clock generator comprises a ring oscillator with an adjustable delay line [9] and an arbitration circuit. Each incoming request for a clock pause (R) is connected to a MUTEX that decides whether to grant the request (AK) or to permit the next clock pulse. The next clock pulse will take place only if all MUTEXes allow it (node B high). Thanks to the C-element, local clock X may be stretched (X+ is blocked) whenever at least one of the incoming R requests is granted (B is low)

while A is rising, and stretching will last until all granted R requests are released (and B goes high). The process is demonstrated in Figure 2.



**Figure 1. Sizable clock generation [1]**

R+ is recognized only when Z=0. Clock cycle stretching occurs when R+ arrives during a stretch window,  $\alpha$ , towards the end of the low phase of Clock Z. If R+ arrives outside the stretch window, port handshake is over in time (B+ precedes A+), causing no stretch. Once a stretch is started, its maximal length is  $\alpha$ . This process can also be described with a timed STG (Figure 3), where the edges are numbered for identification, and the labels on the edges indicate transitions delays. The dashed edge labeled  $\delta$  designates the delay from Z- to R+; observe that certain timing of R+ may make the  $\delta$  edge part of the

critical path, stretching the clock, as follows. Let  $\delta' \in [0, T)$  be the time from Z+ to R+. Since R+ is ignored when Z=1, we define  $\delta$  as the effective time from Z- to a port request, as follows:

$$\delta = \begin{cases} \delta' - \frac{T}{2}, & \frac{T}{2} < \delta' < T \\ 0, & 0 \leq \delta' \leq \frac{T}{2} \end{cases} \quad (1)$$

Note that  $0 \leq \delta < T/2$ . From Figure 3 it can be observed that a stretch occurs if path (6)→(23)→(15)→(16)→(17)→(19)→(21)→(13)→(4) takes longer than a clock cycle:

$$\delta + D_{AC} + D_{MA} + D_{CE} + D_{NOR} > T \quad (2)$$

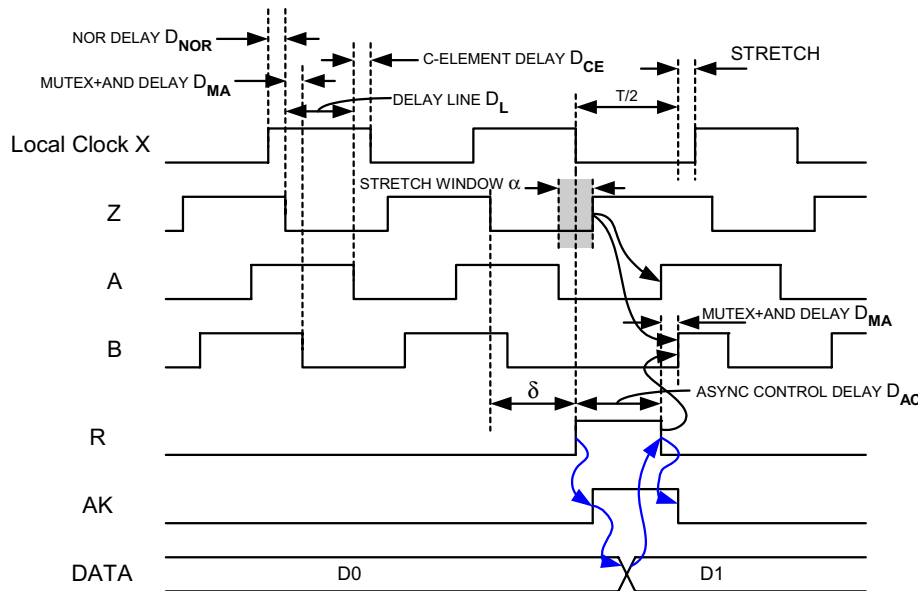
where the various delays are defined in Figure 2. Stated otherwise, the stretch condition is:

$$T - (D_{AC} + D_{MA} + D_{CE} + D_{NOR}) \leq \delta < \frac{T}{2} \quad (3)$$

Subtracting the lower bound from the upper bound, we obtain  $\alpha$ , the size of the stretch window:

$$\alpha = (D_{AC} + D_{MA} + D_{CE} + D_{NOR}) - \frac{T}{2} \quad (4)$$

If the circuit's clock cycle is relatively long, then the clock will never be stretched and parameter  $\alpha$  of Eq. (4) will assume a negative value. For instance, if each of the constant delays in Eq. (4) were 1 ns, operating at slower than 125MHz will guarantee no clock stretching.



**Figure 2. Sizable clock generation – wave diagram**

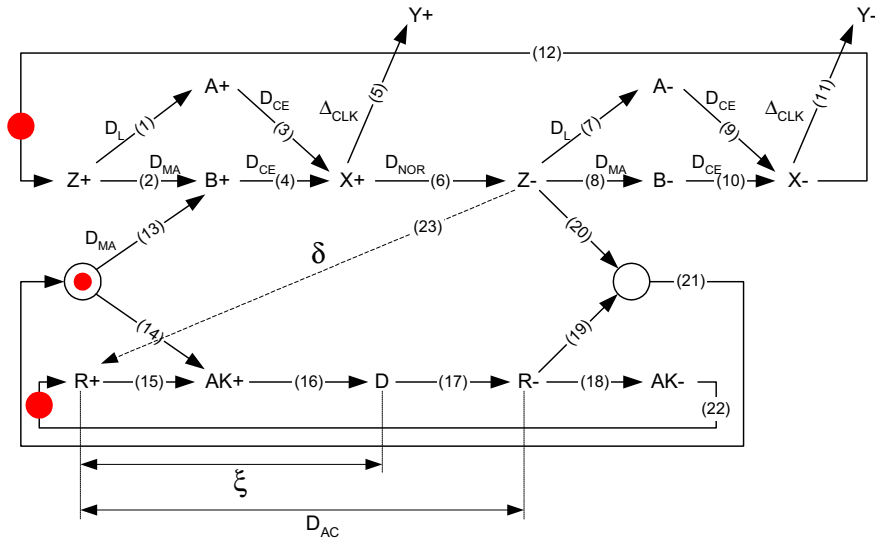


Figure 3. Timed STG of the local stoppable clock of Figure 1

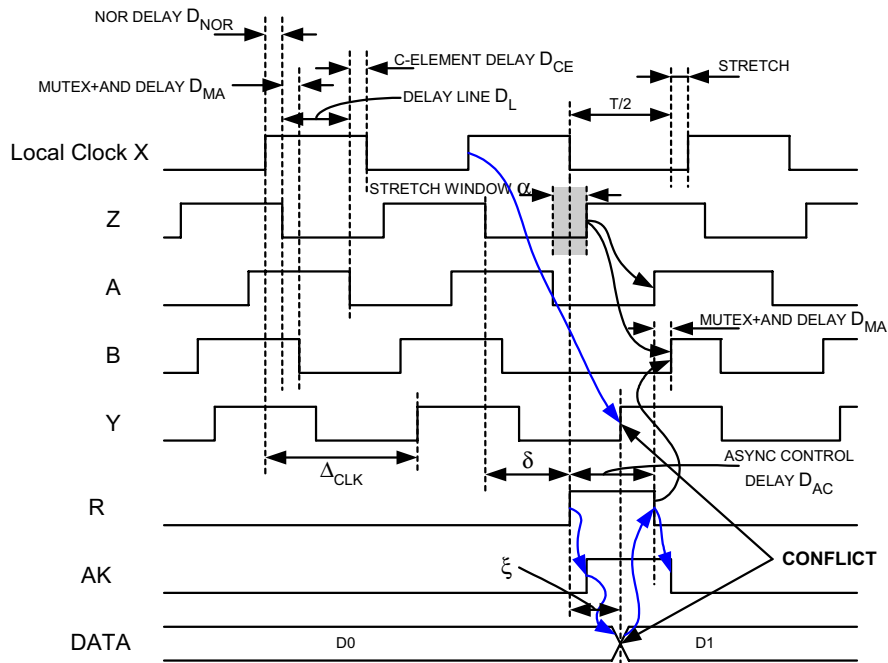


Figure 4. Conflict example

Table 1. Clock tree delays – implementation examples, 0.18μm technology

Design	Clock Frequency	Clock Cycle, T	Clock Skew	Clock Tree Delay
DLX-SYNC (FF)	278 MHz	3.60 ns	60 ps	0.530 ns (15% of T)
DES (FF)	540 MHz	1.85 ns	180 ps	1.168 ns (64% of T)
AES (OpenCores)	350 MHz	2.85 ns	165 ps	1.111 ns (39% of T)
MEM Control (OpenCores)	200 MHz	5.00 ns	126 ps	1.014 ns (20% of T)
Dual Clock MEM Control (OpenCores)	200/100 MHz	5.00 ns	137 ps	1.016 ns (20% of T)

### 3. Synchronization failures in GALS systems

The approach described in Section 2 disregards the delay  $\Delta_{CLK}$  along the clock tree (from node X to Y), thus potentially causing metastability events in the sampling REG of the Locally Synchronous Island (Figure 1). A failure scenario is depicted in Figure 4.

Let's assume that such a request comes  $\delta$  after Z- and is granted by the MUTEX. Uncorrelated with the input handshake, the delayed Clock Y may rise simultaneously with the asynchronous data latching in the Port. The conflict may cause metastability in the input REG of the Synchronous Island. Note that, even though Figure 4 presents the conflict during a stretched cycle, the conflict may happen also when no stretch of the clock occurs, since these two events are not correlated.

In addition to the main problem of metastability, this approach suffers from two other drawbacks: pausing the local clock slows down the entire Synchronous Island, and the slowdown may be exacerbated with multi-port GALS modules, where the probability of pausing the clock is higher.

Starting from X+, the conflict occurs when:

$$\Delta_{CLK} = \delta + \xi + D_{NOR} \quad (5)$$

namely, when the delay along arcs (6)→(23)→(15)→(16) matches the delay along arc (5) in Figure 3. The conflict occurs when Y+ happens inside a "danger window" W (setup+hold time) around  $\delta + \xi + D_{NOR} + k \cdot T$ , where k is an integer ( $k > 0$  accounts for clock delays longer than T). The  $\delta$  statistics is not known, but we believe that the probability of distortion grows with the number of GALS module ports. Figure 5 emphasizes graphically the combinations of  $\Delta_{CLK}$  and  $\delta$  that lead to conflicts. Note that for some values of  $\Delta_{CLK}$ , independent of  $\delta$ , no conflict can happen (regions S in Figure 5). Alternative solutions that avoid such conflicts are described in Section 4.

Clock tree delays depend on both technology and architecture. Clock tree balancing becomes increasingly difficult for high-performance large SoC designs, incurring higher clock tree delays. For instance, in a 0.18 $\mu$ m technology, a typical clock frequency achievable with standard EDA tools and standard libraries is 100–500MHz ( $T=2-10$ ns), while typical clock delays are 1–2ns, depending on module size (some examples are presented in Table 1). Large SoCs, with tens of modules, may require much longer clock delays, approaching T. With faster

technologies and larger chips,  $\Delta_{CLK} > T$  will be a common case if a single global synchronous clock is attempted for the entire SoC. Thus, while  $\delta \in [0, T/2)$ , the range of the clock tree delay is not limited by T.

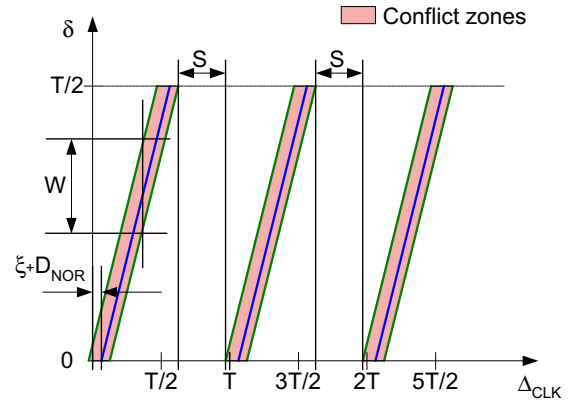


Figure 5. Conflict zones

### 4. Metastability-free GALS clocking

In the following we present metastability-free circuits for data synchronization in GALS modules. The circuits of Sections 4.1 and 4.2 are based on verification of post-layout delays in the original circuit of Figure 1. Section 4.3 analyzes a solution based on standard two-flop synchronizers. Section 4.4 proposes a modification of Figure 1 that avoids metastability at the expense of performance. In Section 4.5, new input and output ports are proposed, replacing the arbitrated clock by locally delayed sampling.

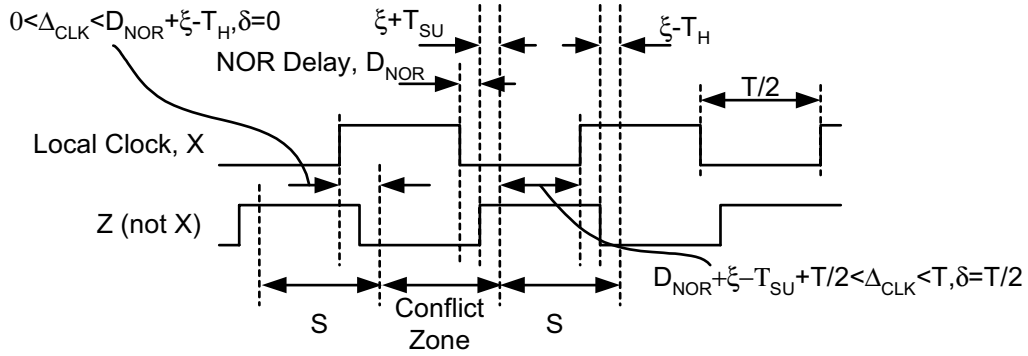
#### 4.1. Limited delay clock tree

When  $\Delta_{CLK} < T$ , it may be possible to verify that a conflict will never occur. This is performed by timing analysis of the physical design and verifying that:

$$\begin{aligned} \Delta_{CLK} &< D_{NOR} + \xi - T_H \cup \\ \Delta_{CLK} &> D_{NOR} + \frac{T}{2} + \xi + T_{SU} \end{aligned} \quad (6)$$

$T_{SU}$  and  $T_H$  are the set-up and hold times of the DFF, respectively. When either rule holds, Y+ will occur only inside the first S region (Figure 5 and Figure 6). The upper bound results from the  $\delta=0$  case and the lower bound from the  $\delta=T/2$  case. Both cases relate to the (6)→(23)→(15)→(16) path in Figure 3.

Note that the relation between  $\xi$  and the clock cycle varies depending on the clock rate and the technology.



**Figure 6. Hazard / no hazard windows example**

This solution suffers from a number of disadvantages. First, it must be verified manually after each layout iteration and clock tree design; the solution is not scalable and it may be sensitive to thermal and power supply voltage changes (different changes in  $\xi$ ,  $T_{SU}$ ,  $T_H$  and  $D_{NOR}$ ). In addition,  $\xi$  is not easy to determine accurately.

#### 4.2. Long delay clock tree

We can generalize the “limited delay clock tree” solution for long delay clock trees having  $\Delta_{CLK} > T$  as follows. The port access is allowed only during the S intervals (Figure 5 and Figure 6). To prevent metastability, the following inequality must be fulfilled:

$$\Delta_{CLK} < D_{NOR} + \xi - T_H \cup$$

$$\left( D_{NOR} + \frac{T}{2} + \xi + T_{SU} + k \cdot T < \Delta_{CLK} \cap \right) \quad (7)$$

$$D_{NOR} + \xi - T_H + (k+1) \cdot T > \Delta_{CLK}$$

Where  $k = 0, 1, 2, 3, \dots$

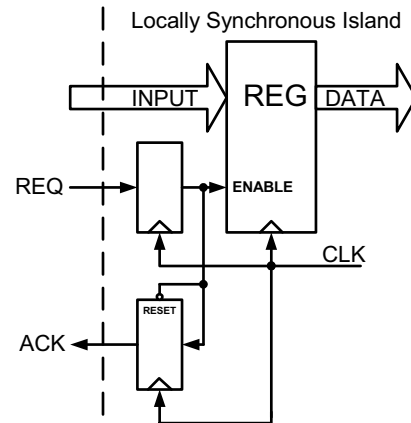
The pros and cons of this approach are similar to the previous one.

#### 4.3. Asynchronous synchronizer

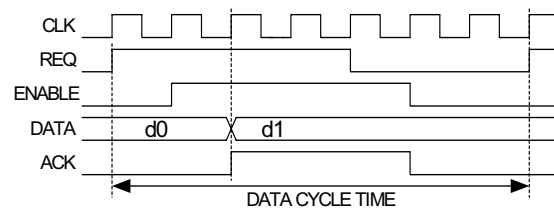
GALS modules may also avoid clock arbitration and employ standard asynchronous synchronizers (Figure 7). The resolving time of the synchronizer should meet MTBF requirements; in Figure 7 we assume that one clock cycle provides sufficient time for metastability resolution. No clock delay verification is required, but the interface data rate is affected drastically (data can not be transferred every cycle).

Assuming mesochronous operation (the same clock frequencies at the transmitter and receiver), the minimal data cycle time ( $REQ^+ \rightarrow REQ^+$ ) takes seven clock cycles in the worst case ( $REQ^+$  happens

immediately following  $CLK^+$  and the transmitter and receiver clocks are in phase), as shown in Figure 8. This data cycle can be reduced when the clocks are out of phase (five clock cycles), or by employing a two-phase protocol (down to three clock cycles).



**Figure 7. GALS synchronization with synchronizer**

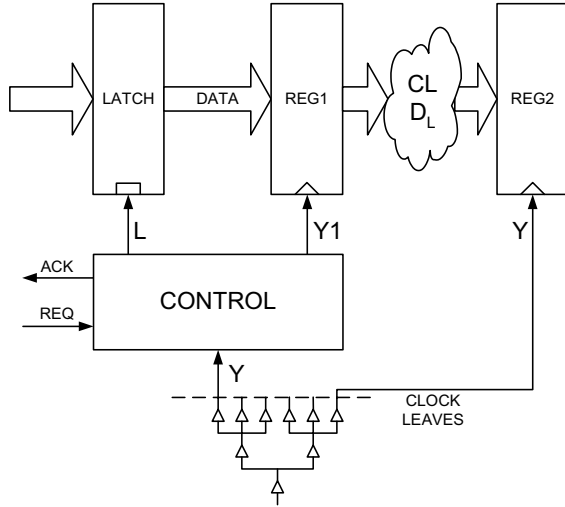


**Figure 8. Data cycle time**

#### 4.4. Matched delay port control

The metastability problem can be solved by inserting delay lines into the circuit of Figure 1, matching the clock-tree delay  $\Delta_{CLK}$ , as shown in Figure 9. Thus we ensure that the handshake will always happen after the clock is stopped.





**Figure 11. Locally delayed latching conceptual circuit**

The worst case of the operation occurs when at the conflict between  $REQ^+$  and  $Y^+$ ,  $REQ^+$  wins. In this case the high-phase of  $Y1$  is maximally shortened (see Figure 12). The implementation must assure that the remaining high phase is long enough, according to the restrictions on the minimal high-phase length by a target library. The contributors to phase reduction are the latency incurred by the asynchronous control,  $D_{CTRL}$ , and the MUTEX resolution latency. We define a minimally allowed high-phase time  $T_{HP}^{Min}$  (typically about three FO4 inverter gate delays). In addition, we define the maximal time that the MUTEX require to resolve metastability,  $T_{Metastab}^{MUTEX}$ .

Then we require that

$$\frac{T}{2} - D_{CTRL} - T_{Metastab}^{MUTEX} > T_{HP}^{Min} \quad (9)$$

$$\Leftrightarrow D_{CTRL} < \frac{T}{2} - T_{HP}^{Min} - T_{Metastab}^{MUTEX}$$

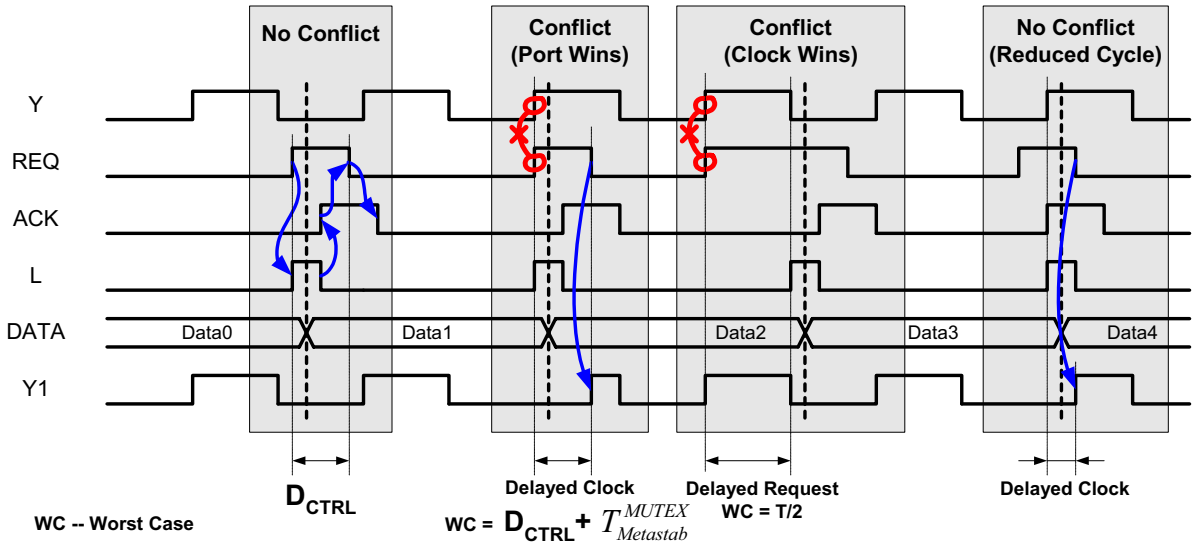
The high-phase reduction is expressed in shortening the whole clock cycle. Therefore, in order to prevent metastability in REG2, the following should be satisfied ( $D_L$  is the latency of the combinational logic between REG1 and REG2):

$$D_L + T_H < T - D_{CTRL} - T_{Metastab}^{MUTEX} \quad (10)$$

$$\Leftrightarrow D_L < T - T_H - D_{CTRL} - T_{Metastab}^{MUTEX}$$

The MUTEX metastability can be tolerated if the clock period is long enough to allow for the resolution of any metastability as well as propagation through the logic that lies in the path to the next register.

Using a standard formula for MTBF [10] and operating at 200MHz with 0.13 $\mu$ m technology ( $\tau=30$ ps and  $W=60$ ps), preserving one quarter of the clock cycle for MUTEX resolution, we obtain MTBF of about 3,000 years. With a 0.35 $\mu$ m technology ( $\tau=100$ ps,  $W=200$ ps and  $F_C=65$ MHz, as used for the simulations in Section 5), the MTBF grows to 10,000 years. For faster operation rate (e.g. 400 MHz at 0.13 $\mu$ m technology) more complicated circuits are required, preserving up to T/2 for MUTEX resolution rather than T/4.



**Figure 12. GALS port synchronization technique – wave diagram**

Preserving one quarter of the clock cycle for MUTEX resolution, Eqs. (9), (10) are updated as follows:

$$D_{CTRL} < \frac{T}{2} - T_{HP}^{Min} - T_{Metastab}^{MUTEX} \quad | \quad T_{Metastab}^{MUTEX} = T/4 \quad (11)$$

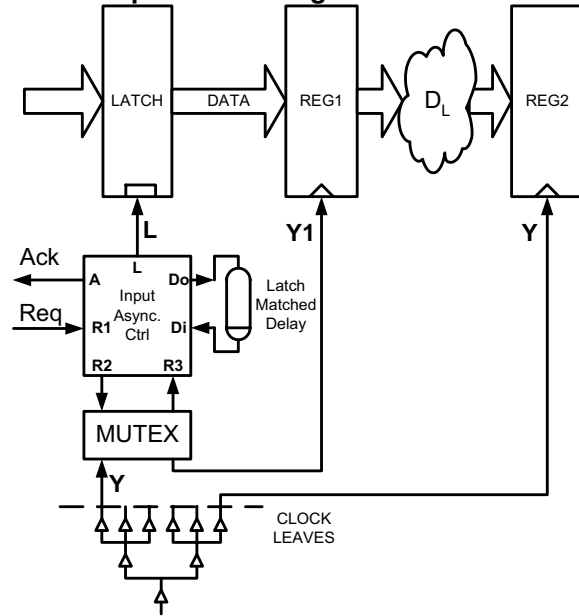
$$\Rightarrow D_{CTRL} < \frac{T}{4} - T_{HP}^{Min}$$

And the logic delay requirement,  $D_L$ , is modified as follows:

$$D_L < T - T_H - D_{CTRL} - T_{Metastab}^{MUTEX} \quad | \quad T_{Metastab}^{MUTEX} = T/4 \quad (12)$$

$$\Rightarrow D_L < \frac{3 \cdot T}{4} - T_H - D_{CTRL}$$

$D_{CTRL}$  contains additional buffering delays when wide data path is required. These constraints are verified in Section 5 for all of the following implementations.

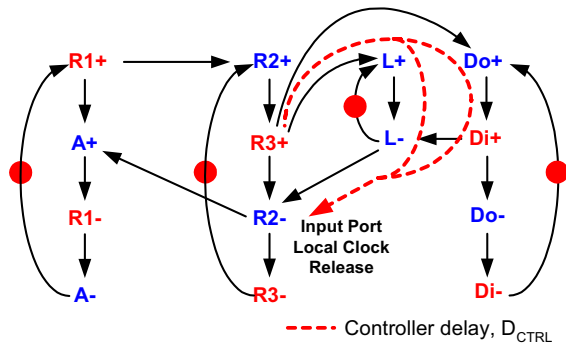


**Figure 13. GALS module decoupled input port**

**4.5.1. Decoupled input port.** Figure 13 shows an implementation of Figure 11. Without a conflict,  $Y1+$  is either not delayed or delayed by less than  $D_{CTRL}$ .  $R2+$  is granted only during the low-phase  $Y$ . The MUTEX arbitrates any conflict between  $R2+$  and  $Y+$ . When  $R2+$  wins over  $Y+$ , the asynchronous controller is granted ( $R3+$ ). The controller employs an asymmetric matched delay  $Do \rightarrow Di$  to open the latch and then close it again ( $L+ \rightarrow L-$ ). After  $R2-$ ,  $Y1+$  triggers REG1, leading to a shortened cycle in the combinational logic following REG1 (the cycle is shortened by  $D_{CTRL}$ ). If the clock wins over  $R2+$ ,  $R3+$

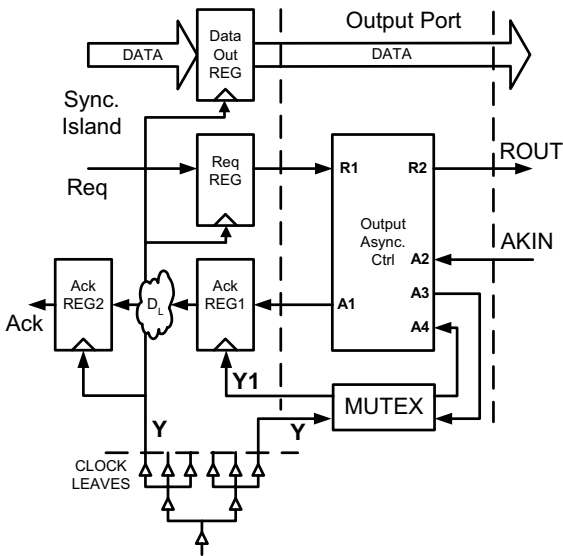
happens only half a cycle later, after Y-. The STG of the Decoupled Input Port control is shown in Figure 14.

The controller delay is measured along the dashed path. The path is contained entirely inside the input port of the synchronous island, thus we ensure that the clock cycle reduction depends solely on the input port control logic (and it does not depend on the logic and clock of the transmitter module). The MUTEX output Y1 should be buffered when wide data path is required. In this case, the additional latency must be taken into account. The latency of the controller is verified in Section 5.

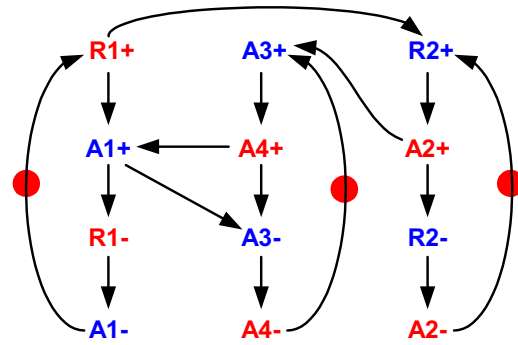


**Figure 14. GALS decoupled input port asynchronous control STG**

**4.5.2. Decoupled output port.** The transmitter circuit is shown in Figure 15. The internal acknowledge (A1) is decoupled from the external asynchronous handshake.



**Figure 15. GALS module decoupled output port**



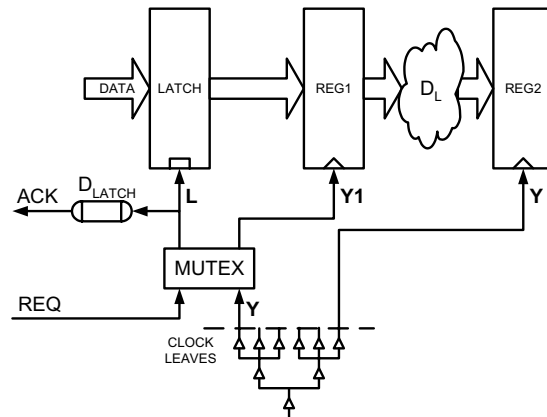
**Figure 16. GALS decoupled output port asynchronous control STG**

The controller latency of the Decoupled Output Port control,  $D_{CTRL}^{OUT}$ , should be verified according to Eqs. (11) and (12). In this case:

$$d_{CTRL}^{OUT} = D[A4+ \rightarrow A1+ \rightarrow A3-] \quad (13)$$

The latency of the controller is verified in Section 5.

**4.5.3. A simpler input port.** The architecture in Figure 17 simplifies the Receiver side, eliminating the asynchronous controller from the Input Port.



**Figure 17. Simple input port**

The receiver delay  $D_{CTRL}$ , now depends on the external delays of the transmitter:

$$D_{CTRL} = D_{LATCH} + D_{TRANSMITTER}(ACK+ \rightarrow REQ-) \quad (14)$$

The Latch Matched Delay (Figure 17) could have been reduced from  $D_{LATCH}$  value to  $D_{LATCH} - D_{TRANSMITTER}$ , but  $D_{TRANSMITTER}$  is unknown a-priori, and therefore it is better to set the Latch Matched Delay to  $D_{LATCH}$ . This simple input port is compatible with the output port of Section 4.5.2. The latency of

this constellation (Simple Input Port with the Decoupled Output Port) is also verified in Section 5.

## 5. Simulations

The circuits of Section 4.5 were synthesized using Petrify [11], converted to VHDL, synthesized by the Synopsis Design Compiler using 0.35 $\mu$ m CMOS libraries, and verified by gate level simulations with wire-load model delays (SDF). Table 2 lists the results for the three controllers.

These results are based on data bus width of 16 bits. In general (and particularly in Table 2), we assume a clock cycle of 160 FO4 inverter delays in a standard ASIC [12]. One quarter cycle is preserved for metastability resolution and another quarter cycle (40

inverter delays) are dedicated to the delay of the asynchronous controller and for high-phase generation. Let's assume that the controller consumes about 25 inverter delays out of the said 40 in the second quarter of the cycle. This leaves 15 gate delays for generating the high phase of the clock. Our 0.35 $\mu$ m library specifies  $T_{HP}^{Min} = 0.361 ns$ , namely about 3 inverter delays. Thus,

$$T_{HP}^{Min} < \frac{T}{4} - D_{CTRL}$$

$\Leftrightarrow$

$$0.361 ns < 1.8 ns = 0.12 ns \times 15$$

as required by Eq. (11).

**Table 2. Controllers delays**

Circuit	Critical Path	Latency (0.35 $\mu$ m)	Num. of FO4 inverter delays	Estimated portion of clock cycle
Decoupled Input Port	R3+ $\rightarrow$ Do+ $\rightarrow$ Di+ $\rightarrow$ L- $\rightarrow$ R2-	3.132 ns	24	15 %
Decoupled Output Port	A4+ $\rightarrow$ A1+ $\rightarrow$ A3-	1.811 ns	13	9 %
Simple Input Port with Decoupled Output Port	Latch Delay $\rightarrow$ A2+ $\rightarrow$ R2-	2.139 ns	14	9 %

According to *Table 2*, the delays of all three asynchronous controllers are lower than the bound of 25 FO4 gate delays. This margin allows operating at a slightly higher frequency, if needed. Evidently, this approach is limited by the time we reserve for the MUTEX to resolve. However, it provides a useful operational frequency range for most ASICs.

## 6. Conclusions

Previously proposed locally generated, arbitrated clocks for GALS SoCs [1][5][6][7] face the risk of synchronization failures if clock delays are not accounted for. The problem has been analyzed based on clock delays, cycle time, and complexity of the asynchronous port controllers. A few methods have been presented. First, we have examined what analysis should be carried out to verify known solutions (using arbitrated clocks) in the presence of clock delays. Second, we have discussed the use of various synchronizers. Simple synchronizers may be used when high data bandwidth is not required. Another variation is based on employing matched delays, where a control signal is delayed so as to match the clock delay and avoid synchronization failures. Arbitrated clocks may be traded off for locally delayed input and

output ports, facilitating high data rates. We have described three such ports, two for input and one for output. The three circuits have been simulated and have been shown to eliminate the need for stopping the clock under certain conditions.

As SoCs become more complicated and as clock delays inside GALS modules become longer, these methods will have to be developed even further. The feasibility and attractiveness of large and fast GALS SoCs depend on minimizing the synchronization overhead.

## 7. Acknowledgment

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