A Mixer Frontend for a Four-Channel Modulated Wideband Converter with 62 dB Blocker Rejection

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***Abstract*—The Modulated Wideband Converter promises to improve receiver flexibility for cognitive radios by leveraging compressive sensing techniques. We present a prototype IC that adds signal reception to previously demonstrated signal detection. Refactoring the mixing sequence between detection and reception enables targeted reception and blocker rejection. We algorithmically design a three-level mixing sequence and additionally employ delay-based harmonic cancellation. When applied together in our 65-nm chip, we measure 62 dB of in-band blocker rejection, while receiving up to four channels between 0 and 900 MHz.**

***Index Terms*—Cognitive radio, harmonic rejection mixer, modulated wideband converter.**

I. Introduction

Frequency-agile radios are an active area of research and receivers based on compressive sensing (CS) are one of the options being considered for future systems [1-3]. Among the different variants of CS receivers, the modulated wideband converter (MWC) [4] is architecturally close to a bank of direct conversion receivers and is hence attractive for CMOS realization. In [5], a variant of the MWC was employed for wideband spectrum sensing and interference detection. In this work, we report a frontend for the MWC that supports signal reception for up to four channels. Unlike conventional receivers, the MWC can adjust the number of bands it receives, and is agnostic to their locations, making it a particularly attractive architecture for cognitive radio.

A key feature of the presented frontend is that, unlike previous incarnations, it can attenuate a single in-band blocker by 62.8 dB, or two blockers by 50.2 dB. As described below, we achieve this through two complimentary techniques that may be used in concert or applied independently—algorithmic three-level digital mixing sequence design and a parallel harmonic cancellation mixer path. The latter is enabled by a background-calibrated digital-to-delay converter (DDC) with a step size of 1.2 ps, which leverages the fine time granularity of modern CMOS.

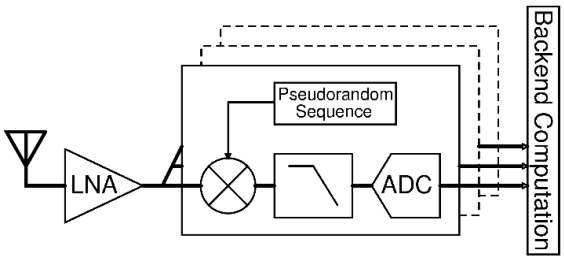


Fig. 1. The MWC architecture as described in [4]

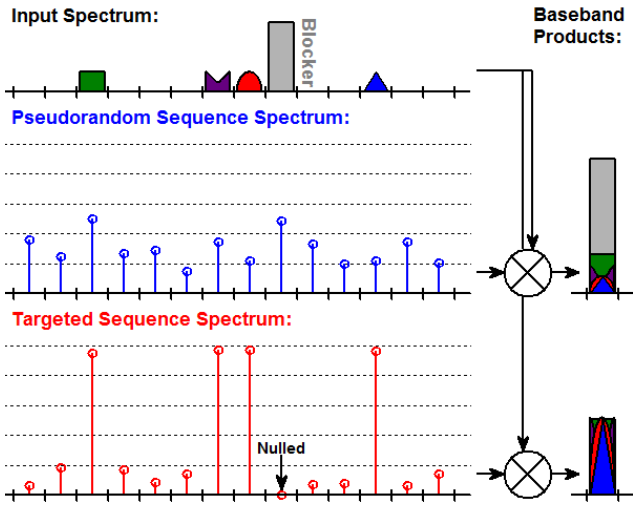


Fig. 2. Pseudorandom vs. targeted missing sequence (which provides blocker rejection and noise attenuation).

II. Detection and Reception in the MWC

The MWC architecture, introduced in [4], is depicted in Fig. 1. Previous work used a spectrally rich pseudorandom sequence to guarantee that power from each input band is mixed to baseband. However, a pseudorandom sequence provides no blocker rejection (see Fig. 2) and incurs a severe noise penalty, since the effective noise bandwidth spans the entire spectrum. In this work, we note that after the detection algorithm determines the frequency support, that information can be used to design a targeted mixing sequence. By maximizing the desired signal harmonics and nulling a strong blocker harmonic we provide blocker rejection and improve the signal-to-noise ratio (Fig. 2).

III. Sequence Design and Harmonic Rejection (HR)

Once the detection step has determined the signal locations, we compute a suitable mixing sequence off chip. This is done by summing a set of sinusoids, each centered in a target band, and quantizing the result. We add additional flexibility to the sequence design by extending the set of possible mixing coefficients from ±1 to include 0, which we use to reject an identified blocker band. A

greedy algorithm adjusts a small fraction of the zero-level elements to null the undesired harmonic. Since quantization nulls those sequence elements that do not strongly contribute to the desired harmonics, those that do remain unchanged. Furthermore, the additional zero-level enables a more accurate quantization and thus reduces the out-of-band noise folding by about 3 dB.

In addition, we include a parallel mixing branch that is driven by an identical, but delayed copy of the mixing sequence. By precisely setting the delay, an undesired mixer harmonic can be rotated by $k\pi$ radians. For odd k, summing the original and delayed copies presents a comb filter to the mixer harmonics with a notch that is designed to fall on the undesired harmonic. The comb filter gain is given by $2\cos(2\pi\omega k/nT)$, where T is the mixing sequence period and n is the undesired harmonic. Increasing k increases the frequency at which notches in the comb filter occur and decreases the bandwidth of each notch from 900 to 1.5 MHz. We choose k to minimize the attenuation of harmonics that correspond to desired signal bands.

The maximum possible sequence-based HR is limited by our ability to null the undesired harmonic, due to the finite number of ways the zero-level sequence elements can be adjusted. Delay-based HR is bounded by mismatch. In addition, both HR techniques are sensitive to jitter (see Fig. 3). When we apply both techniques to the same blocker, they compound, greatly reducing the jitter corner.

IV. Circuit Implementation

We designed an IC to demonstrate the ability of the MWC to compete with traditional receiver architectures in noise performance and single blocker rejection. To simplify the design, we limited the scope of the chip to the critical core circuitry. In the MWC, the key circuit block is the mixer. On chip, we thus implement data storage for the mixing sequence, the digital-to-delay converter, the mixer itself, and its subsequent anti-alias filter. We leave the LNA, VGA, and ADC off chip (see Fig. 4).

a) Mixing Sequence Data Storage: Each mixing sequence is computed off chip and stored on chip in two closed-loop shift registers of length 1332, which run at 1.85 GHz. The clock rate is set by the Nyquist frequency of the input spectrum, and the sequence length is set by the desired channel bandwidth. We chose shift registers to facilitate debugging, however, as each shift register stores the same data, future implementations may use a single shared SRAM to save power and area.

Our chip is designed to recover one to four signals between 0 and 900 MHz, and has three bandwidth modes, which are achieved by adjusting the effective length of the mixing sequence; 1.4 MHz with a 1332 element mixing sequence, 2.8 MHz with a 666 element mixing sequence, and 4.2 MHz with a 444 element mixing sequence. Recovering higher input frequencies is difficult for the MWC, because both clock frequency and sequence length scale with input frequency. However, higher frequency inputs can be received (as in [5]) by adding an IF mixer.

b) Digital-to-Delay Converter (DDC): The harmonic cancellation delays span the entire period of the mixing sequence, and so the DDC is implemented in a coarse-fine architecture. Coarse delay control is provided by delaying the sequence the appropriate number of clock cycles within the shift register. Fine control is implemented in a digital delay line with adjustable load capacitors (see Fig. 5(a)). The DDC capacitors are implemented with deep n-well MOS devices and the total extracted per-stage capacitance ranges between 470 aF and 28.2 fF. The DDC allows control of the mixer transitions with 1.2 ps resolution anywhere within the 540 ps clock period.

c) Mixer Implementation: Both the calibration switches and the three-level current-mode passive mixer are folded into the same circuit block depicted in Fig 5(b). The input resistors set the input impedance match, and the calibration switches allow for measurement of the calibration tone. We implement the mixer's zero-level by adding switches that tie both the input and output ports of the mixer to common mode. In this state there is no transmission across the mixer and we add resistors so that both ports see a first-order impedance match.

d) Anti-Alias Filter: The filter is implemented as an active RC design using a two-stage amplifier (see Fig. 5(c)). The op-amp's virtual ground is used for summing the currents of the mixers and its delayed copy.

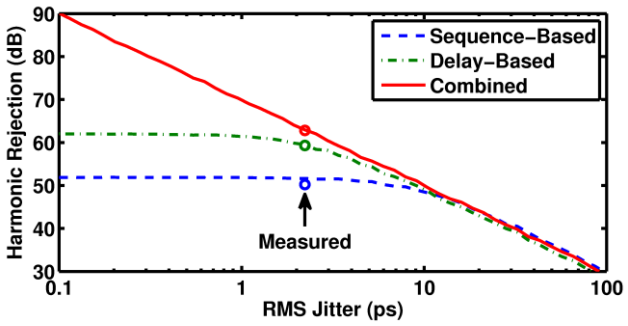


Fig. 3. Simulated HR vs. jitter (with 3% delay path mismatch)

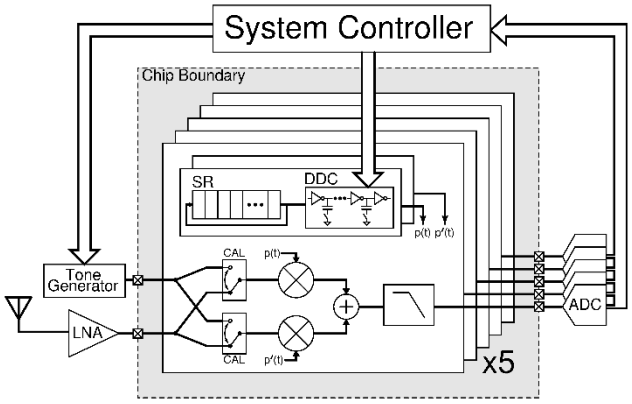
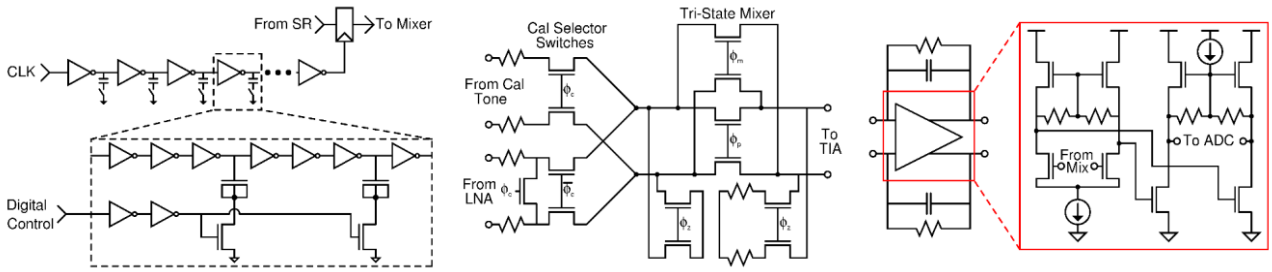


Fig. 4. Test setup and chip architecture



(a) (b) (c)

Fig. 5. Simplified schematics of key circuit blocks (a) digital-to-delay converter (b) mixer (c) anti-alias filter

e) Calibration: As shown in Fig. 4, the chip contains five identical branches, one of which is used for background calibration, which proceeds one branch at a time. The calibration branch matches its mixing sequence delays to those of an active branch. Then, calibration switches are toggled so that the calibration branch substitutes for the active branch. The active branch is removed and fed with a sinusoid in the blocker band that we generate off chip. Next, the DDC code is swept and the baseband power of the calibration tone is measured. The code that minimizes that power is selected and the now-calibrated primary branch is switched back into the signal path. Calibration then proceeds with the next branch. Since the delay-based cancellation rejects all odd multiples of the target harmonic, a square wave generator can be considered as the test signal in future work.

V. Measurement Results

Fig. 6 depicts the calibration tone power near the optimal digital delay. The difference in measured tone power between the expected code and calibrated code demonstrates both the need for calibration and its efficacy. The measured harmonic rejection is shown in Fig. 7, wherein we apply two equal-power test tones, one in a blocker band and one in a signal band (in this case 878 and 881 MHz respectively). At baseband, we measure the down-converted power for both tones—the difference corresponds to the achieved harmonic rejection. We demonstrate 50.2 dB of sequence-based rejection, 59.3 dB of delay-based rejection, and 62.8 dB with both applied to the same blocker. Furthermore, we note that the measured rejection for each scheme closely matches the simulation presented in Fig. 3 with an estimate of 2.2 ps RMS clock jitter.

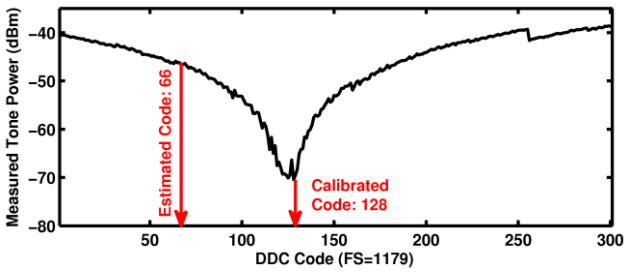


Fig. 6. DDC calibration sweep

Fig. 8 demonstrates the back-end signal recovery of the MWC. We drive the MWC with sinusoids in four bands spread across the input spectrum and recover those bands from the baseband samples of each branch. By appropriately setting the branch-branch mixing sequence, we ensure linearly independent baseband measurements. We recover the input signal by inverting a matrix of complex mixer harmonics and multiplying it with the frequency-domain baseband measurements [4]. Our system demonstrates 37 dB of band-band rejection, which is limited by the accuracy with which we estimate the complex mixer harmonics.

Our mixer shows 64.8 dB of IIP2 and 14.3 dB of IIP3. We measure the IIP2 by applying a 300 MHz tone to the input and using a mixing sequence designed to target both the 300 MHz and 600 MHz bands, thus directly capturing the second harmonic distortion of the mixer. We measure the IIP3 by applying two-tones separated by 150 kHz in the 500 MHz band. We measure a per-channel noise figure of 37 dB using direct application of the Y-factor method and factoring out the effects of peripheral devices using Frii's formula. However, the MWC makes an independent measurement of the incident signal in each of its branches so in a fair comparison to standard topologies

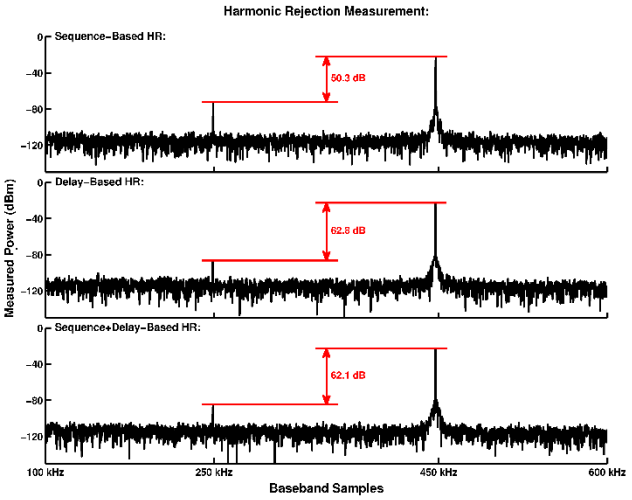


Fig. 7. Harmonic rejection measurements

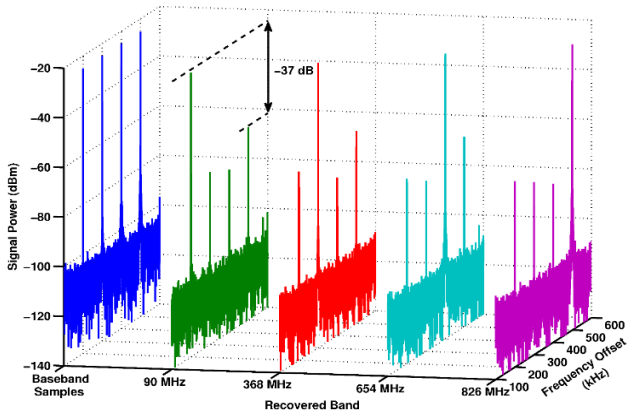


Fig. 8. Measured recovery of the four baseband signals using the output data from four channels.

we see a 6 dB noise figure improvement due to averaging.

Adding a hypothetical LNA with 2.5 dB NF, 0 dBm IIP3, 26 dB gain, and applying cascading relationships yields an overall system with 10 dB of SNDR at -25 dBm input power and -96.5 dBm of sensitivity. Accounting for the 3 dB SSB noise penalty and a 0.5 dB increase in signal bandwidth, these results closely parallel the LTE specifications for 5 MHz bandwidth signals up to 900 MHz, and a survey of recent work demonstrates that these specifications are achievable for wideband LNAs [9-10]. Furthermore, our mixer's performance is competitive with recently published architectures (see Table I) that do not demonstrate the flexibility of our design.

The per-branch power draws for the mixer+TIA, DDC, and shift register are 22.8 mW, 3.8 mW, and 149.5 mW, respectively, from a single 1.2V supply. The entire chip occupies 3.84 mm^2 and is implemented in a 65 nm CMOS process. The per-branch active area is 0.0845 mm^2, split between the shift registers (0.0376 mm^2), DDCs (0.00317 mm^2), TIA (0.0402 mm^2), and mixer (0.00349 mm^2). The rest of the area is used for decoupling capacitors and guard rings. An annotated die photo is provided in Fig. 9.

TABLE I

COMPARISON TO RECENT HARMONIC REJECTION MIXERS

	[6] Rafi	[7] Sundström	[8] Yang	This Work
System	HR IF mixer	Dual-carrier aggregation IF HR mixer	Wideband single-channel mixer for SDR	Multi-channel mixer for detection and reception
Tech (nm)	110	65	45	65
Area/Branch (mm^2)	0.034	0.48	0.352	0.085
Supply voltage (V)	2.7 (mix) 1.3 (clk)	1.2	1	1.2
Min HR (dB)	52	68	55	62.8
IIP2 (dBm)	>75	-	-2	64.8
IIP3 (dBm)	12	-	-3	14.3
NF (dBm)	11 (DSB)	-	35 (SSB)	31 (37-6, SSB)
Signal Path Power/ Branch (mW)	59.4	23.6	17	22.8+3.8
Frequency (MHz)	100-300	390	500-1500	0-900

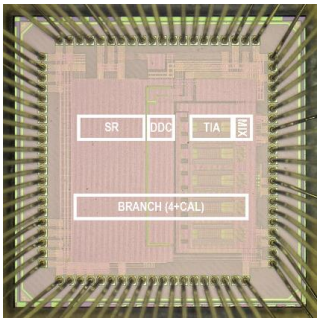


Fig. 9. Die photo

VI. CONCLUSIONS

The MWC is a promising circuit architecture for cognitive radio applications because it can quickly determine the spectrum characteristics [5] and dynamically adjust the number and bandwidth of its reception channels across a wide frequency range [4]. In this work we add two topology improvements to the MWC that provide blocker rejection and sensitivity comparable to traditional receiver architectures while maintaining the flexibility advantage of the system.

ACKNOWLEDGEMENTS

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