1/\( f \) noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation

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A new experimental setup for the study of 1/\( f \) noise of metal-oxide-semiconductor transistor under nonsteady state conditions is presented. The noise measurements demonstrate for the first time that, by interposing periods of negative bias corresponding to accumulation between the monitored periods of positive bias corresponding to inversion, the low-frequency noise sampled in the positive bias intervals is reduced.

1/\( f \) noise phenomena in electronic devices have been extensively investigated over the past 50 years. Yet it seems that in spite of numerous experimental and theoretical studies, the physical mechanism and origin of the 1/\( f \) noise is still not fully established. The most widely accepted theory at present, for metal-oxide-semiconductor (MOS) transistors, is charge trapping–detraping models which assume a distribution of trapping times that arise from the transition of electrons from the semiconductor surface to traps located in the oxide. 1–8 1/\( f \) noise is characterized by its power spectral density and its long correlation time. The physical process that is responsible for the 1/\( f \) noise has a "long time memory." 9,10

According to the trapping models of 1/\( f \) noise in a MOS transistor, the power spectral density is obtained by a superposition of relaxation processes with Lorentzian spectra and a distribution of time constants. A superposition of Lorentzian processes can give rise to a spectrum which varies inversely with the frequency. An appropriate distribution of time constants is required to give the 1/\( f \) law over an extensive range of frequency. In order to extend this to ten decades, the spread in time constants must cover many orders of magnitude. In the MOS transistor, it is possible to invoke a physical mechanism (trapping) which could account for relaxation times distributed between, say, \( 10^{-5} \) and \( 10^8 \) s. 9,10

McWhorter suggested that such a distribution of trapping times at a semiconductor-oxide interface could arise from a spatially uniform distribution of tunneling depths to traps in the oxide. 2,4 More recently, Dutta and co-workers have demonstrated that activated processes with a broad distribution of activation energies explain the 1/\( f \) noise observed in continuous metal films 5,6. The same approach has been adopted by Ralls et al., who have demonstrated that interface traps in submicron MOS transistors are characterized by a wide range of activation energies. Each trap exhibits a Lorentzian spectrum and the distribution of time constants yields a power spectrum proportional to 1/\( f \). In a recent paper, Fleetwood and Scofield have linked the traps to oxygen vacancies in the SiO\(_2\) layer. 8 According to the above trapping–detraping models, the "long time memory" of the processes that produce the 1/\( f \) noise is associated with the long occupation time constants of the traps.

This letter addresses the following question: is it possible to interfere with the self correlation of the physical noisy process and thereby reduce the noise by a rapid switching between two states—one state that is characterized by a significant generation of 1/\( f \) noise and another state that is characterized by a negligible amount of 1/\( f \) noise. In spite of the straightforward question, conflicting and opposing predictions can be speculated.

The experiment is performed with a silicon surface MOS transistor that produces extensive 1/\( f \) noise when the gate is biased into inversion and the transistor is "on" and exhibits negligible 1/\( f \) noise when the gate is biased into accumulation and the transistor is "off."

The MOS transistor is switched between the two states and sampled at the "on" state for low-frequency noise measurements. The "off" states introduced between the noisy "on" states are expected to reduce the low-frequency noise by interfering with the long time constants associated with trapping and detraping processes, and hence with the long time memory that characterizes 1/\( f \) noise.

This letter describes the experimental setup for the study of 1/\( f \) noise measurements of MOS transistors under switching conditions between two states with different noise behavior. The noise measurements indicate that by interfering with the slow transition of electrons by switching from accumulation to inversion, the 1/\( f \) noise power that is sampled when the gate bias is "on" is reduced.

Figure 1 describes the electronic circuit that measures the 1/\( f \) noise of n-channel MOS transistors under switching conditions. The MOS transistor under test is switched between two states. In state 1 the gate voltage is positively biased to \( V1 \) and the MOS transistor operates in the ohmic region. In this state, the drain voltage is amplified, filtered, and sampled. The output of the sample-and-hold circuit is connected to a Dynamic Signal Analyzer (model HP 3562A) which measures the spectrum of the noise. In state 2, the gate voltage is biased to accumulation \( (V2) \) to interfere with the mechanism that generates the 1/\( f \) noise.

The drain is connected to an adjustable, low-noise dc current source and the source is connected to a variable low-noise negative dc voltage \( (V3) \). The drain potential is always zero because in state 1 the drain current \( I_d \) and the voltages \( V1 \) and \( V3 \) dictate it, and in state 2 the drain is connected via an electronic switch to the ground in order to prevent saturation of the amplifier when the MOS transistor is "off."

The role of the low pass filter (LPF) is to prevent aliasing due to sampling. The switching frequency is 600
FIG. 1. (a) Schematic diagram of the electronic circuit designed for the study of 1/f noise measurements of MOS transistors under nonsteady state conditions. The MOS transistor is switched between two states: state 1 (determined by V1) that is noisy, and state 2 (determined by V2) that is not noisy. The noise voltage at the drain is amplified, filtered, and sampled at the noisy state. (b) Vg switches the gate bias Vgs between state 1 where the MOS transistor conducts and generates considerable 1/f noise at the drain, and state 2 where the MOS transistor is cut off. Vb connects the drain to ground at state 2 in order to avoid saturation of the amplifier. V1, V2, and V3 are low-noise adjustable dc voltage sources that determine the operation point of the transistor.

Hz and the cut-off frequency of the LPF is 3000 Hz which is high enough to prevent signal and noise reduction due to the combined action of the LPF and the sample-and-hold circuits. This design does not conform to the Nyquist law and some aliasing does appear at the higher frequencies, but it is small due to the 1/f dependence of the spectrum.

Numerous noise calibration measurements were performed to ensure that the MOS transistor is the dominant noise generator in the circuit. Voltage gain from gate to output was measured and checked to be the same for a constant gate bias of V1 as well as for the switched gate bias, which indicates that the observed noise reduction is due to physical phenomena and not due to the electronic circuit.

Figure 2 exhibits the noise spectrum as measured in the signal analyzer. The upper curve (a) measures the noise voltage spectral density for V1 = V2. Vgs is constant and the MOS operates in the ohmic region. The operation point of the MOS transistor is given in the figure caption. The switching action of the drain does not affect the MOS operating conditions. The measured noise spectrum [curve (a)] is identical to the one measured in the dc state without any switching and sampling actions.

Curve (b) exhibits the measured noise spectrum for the case in which the gate of the MOS transistor is switched between inversion and accumulation. A reduction by a factor of 3 in the noise power at 1 Hz is observed.

Figure 3 exhibits the noise reduction at 1 Hz as a function of Vgs in a switching mode of operation. The gate voltage in state 1 is biased to impose conduction, and Vgs varies between inversion, where the transistor conducts, and strong accumulation where the transistor is cut off. The dependence of the drain current (Ids) upon the gate voltage (Vgs) is also exhibited.

Figure 3 indicates that in order to reduce the 1/f noise by interfering with the physical noisy process, state 2 must establish a significant change in the Fermi level at the surface and hence in the occupation of the trapped carriers, as compared with state 1 in which the noise is sampled. It

FIG. 2. Noise voltage spectral density at the output of the electronic circuit: (a) for V1 = V2 = 5 V the gate bias Vgs is constant and the MOS transistor operates at the ohmic region. (b) the gate voltage is switched between V1 = 5 V, which imposes inversion and hence conduction, and V2 = -3 V, which imposes accumulation and hence cut off. A reduction by a factor of 3 in the noise power at 1 Hz and a change in the shape of the curve is observed.

FIG. 3. (Dots) The relative reduction S0/Sn in the noise power spectral density at 1 Hz as a function of the gate voltage at state 2. (Solid line) The drain current as a function of gate voltage. Threshold, midgap, and flatband voltages are Vth = 0.8 V, Vfb = 0.1 V, and Vfb = -0.85 V, respectively.
decades between state 1 and state 2, the noise power is nearly unaffected. Only when state 2 imposes surface potential that corresponds to midgap and towards accumulation does a significant reduction in the noise power occur.

The observed reduction in the noise amplitude is found to be practically independent of the relative fraction of the switching time in which the MOS transistor is in state 2, for a fraction between 0.12 and 0.75.

Figure 4 exhibits the spectrum of a simultaneous signal and noise measurement: \( V_1 \) consists of a low-noise dc voltage and an ac signal at 5 Hz with an amplitude of 10 \( \mu \)V superimposed on the dc component of \( V_{g1} \). In curve (a) the dc component of \( V_{g1} \) and \( V_{g2} \) are equal to 3.5 V (conduction). In curve (b) the MOS transistor is switched between \( V_{g1} \) and \( V_{g2} \) that imposes accumulation and hence cut off. The switching mode of operation does not reduce the signal but affects the 1/f noise.

It is interesting to note that for \( V_{gs2} = 0.6 \) V (below threshold voltage) and a drain current that is reduced by two orders of magnitude, the low-frequency noise is reduced by a factor of 3 at 1 Hz. The residual 1/f noise component that is not affected by the switching mode of operation may be contributed by additional noise mechanisms in the MOS device which are not affected by the switching mode of operation.

In conclusion, a reduction in the 1/f noise amplitude is obtained by switching the device between two states: one state that generates a considerable amount of 1/f noise and an additional state that produces a negligible amount of 1/f noise. The experiment demonstrates the following major point: interposing negative periods correspond to accumulation between the monitored periods of positive bias corresponding to inversion, the low-frequency noise sampled in the positive bias intervals, is reduced. The fact that the outcome of the experiments is not predicted with an established theoretical ground enlightens the significance of the experiments.

The experiment described in this letter interferes only with the time constants that are in a limited range corresponding to the switching rate and these are only a small fraction of the overall time constants. Hence, the experiment demonstrates that by cycling from inversion to accumulation the 1/f noise power is reduced, but only by a relatively small factor. The residual 1/f noise component that is not affected by the switching mode of operation may be contributed by additional noise mechanisms in the MOS device which are not affected by the switching mode of operation.

It will be worthwhile to repeat the experiment of switching between two states, a "noisy" state and a "noiseless" one and to observe the effect of the interference with the physical process with additional devices. For example, to switch a diode between high reverse bias characterized with a large amplitude of 1/f noise and zero bias which does not produce 1/f noise and to measure the effect on the 1/f noise.

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