Low noise CMOS readout for CdZnTe detector arrays

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Abstract

A low noise CMOS readout for CdTe and CdZnTe X- and gamma-ray detector arrays has been designed and implemented in the CMOS 2 $\mu$m low noise analog process provided by the multi-chip program of Metal Oxide Semiconductor Implementation Service. The readout includes CMOS low noise charge sensitive preamplifier and a multiplexed semi-Gaussian pulse shaper. Thus, each detector has a dedicated charge sensitive preamplifier that integrates its signal, while a single shaping amplifier shapes the pulses after the multiplexer. Low noise and low-power operation are achieved by optimizing the input transistor of the charge sensitive preamplifier. Two optimization criteria are used to reduce noise. The first criterion is based on capacitance matching between the input transistor and the detector. The second criterion is based on bandwidth optimization, which is obtained by tailoring the shaper parameters to the particular noise mechanisms of the MOS transistor and the CdZnTe detector. Furthermore, the multiplexing function incorporated in the shaper provides low power and reduces chip area. The system is partitioned into a chip containing the charge amplifiers and a chip containing the semi-Gaussian pulse shaper and multiplexer. This architecture minimizes coupling from multiplexer switches as well as shaper output to the input of the charge sensitive preamplifiers. © 1999 Elsevier Science B.V. All rights reserved.

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1. Introduction

Multi-channel X-ray and gamma-ray spectroscopy with good energy resolution is highly required in the area of nuclear medicine imaging systems. Good energy resolution is useful for suppressing gamma-rays that have undergone Compton scattering. Semiconductor detectors are attractive for use in nuclear medicine because they have adequate energy resolution and allow small and reliable systems. Silicon and germanium are excellent semiconductor detectors but neither is practical for nuclear medicine due to the low gamma-ray stopping power and the requirement of costly cryogenics. Among the room-temperature semiconductor detectors, HgI$_2$ and CdTe [1] have been considered for use in gamma cameras. Recently, CdZnTe [1] has become the most attractive candidate, because of its superior spectral performance [2].
The current trend in high-energy physics and other disciplines that require ionizing radiation detectors, is toward smaller pixels and a large number of channels. These systems should provide better position resolution and low noise performance. This has motivated the development of integrated circuits that provide the readout electronics. CMOS technology is used for the implementation of those integrated circuits, because of the low-power consumption and the ability to build small, high gain voltage amplifiers, accurate capacitors and switches.

This work focuses on the development of a low-noise CMOS readout for a CdZnTe imaging array that can serve as a modular building block for nuclear medicine imaging systems. We also report here of a novel multiplexer design, which significantly reduces the number of shaping amplifiers and additional parts of the analog readout channels. This system is described in Section 2.

Low noise and low power are achieved by optimizing the charge sensitive amplifier and detector. Two optimization criteria are used. The first criterion is based on capacitance matching between the charge sensitive preamplifier and the detector. The second criterion is based on bandwidth optimization, which is obtained by tailoring the shaper parameters to the particular noise mechanisms of the MOS transistor, including 1/f noise, and the CdZnTe detector noise. The charge preamplifiers together with the noise optimization procedure are presented in Section 3.

2. The readout integrated circuit

A simplified schematic of the analog Multiplexer (MUX) readout is shown in Fig. 1. The system is partitioned into a chip containing the Charge Sensitive Preamplifiers (CSP), and a chip containing the MUX and the rest of the analog channel. This architecture minimizes possible parasitic coupling from the shaper output to the CSP inputs. In future implementations the detectors array will contact the CSPs array by using indium bumps [3]. Each detector is AC coupled to its CSP to avoid the preamplifier saturation by detector DC currents. The preamplifier is a switched capacitive feedback transimpedance amplifier, implemented by CMOS technology [4]. The total capacitance at the input of the CSP must be as small as possible in order to reduce the total noise of the analog channel, as explained in the next section.

A series capacitor C (~ 180 pf) and a switch S follow the output of the CSP. When this switch is closed, during the read operation, a ‘CR’ derivative is formed, which is the first part of a CR–RC semi-Gaussian pulse shaper amplifier, where RC is the shaping time of the shaper. Following the MUX an integrator common to all the channels completes the second part of the shaping function (see Fig. 1).

The analog switch S is implemented by minimum size CMOS pass-transistors that have a low ‘on’ resistance compared to R. Nevertheless it also has parasitic capacitances (gate-source and gate-drain capacitances) which might cause cross-talk and charge injection during MUX operation [7]. In order to minimize these effects both n-channel and p-channel transistors are used to implement the switch.

The read operation follows a polling method. When it reads the nth channel by setting the appropriate address, all the other S switches remain open. If another detection event happens at the same time in a different channel, the information of the induced charge is stored in the feedback capacitor of
the CSP. Since there is no discharge path, this information is stored until the next read. If two or more events take place at the same channel before the read, an error occurs. For example, let us assume source activity of 25 μCi detected by 2 × 2 mm pixels in a distance of 40 cm and the processing time per channel is 20 μs. Then one analog MUX will be able to handle the readout of up to ~2000 pixels (~45 × 45 detectors).

After the detection event, a step voltage occurs at the feedback capacitor, while the voltage at C is kept constant. During the read, the capacitor C is charged according to the new voltage, and the S voltage is restored to zero. A voltage pulse at the integrator accompanies the charging process at C, which is the signal for the next stages. The peak of the integrator pulse is locked by the peak detector, and is A/D converted. In parallel, a comparator provides the ‘ready’ signal to the controller. The controller stores the information in the address corresponding to the energy of the detected photon, providing the channel spectrum. The ‘Acknowledge’ signal resets the peak detector for the next measurement, and the controller moves to the next channel. If, however, the ‘Ready’ signal is not activated, then the controller clears that channel (‘Acknowledge’) and immediately moves to the next channel. Fig. 2 shows the schematic waveforms of the readout algorithm.

3. CSP and noise optimization [4–8]

A CMOS operational amplifier, a feedback capacitance and a CMOS switch form the CSP used in the preamplifier array chip. The CSP and the noise optimization method have been presented in Ref. [4]. Fig. 3 shows the preamplifier small signal circuit and noise sources used for the noise analysis. The small signal elements considered are the detector capacitance $C_{det}$, the amplifier input capacitance $C_{inp}$, the parasitic capacitance due to connections $C_p$, and the feedback capacitance $C_f$. The noise sources considered are the amplifier 1/f and thermal noise $S_{Va} = S_{Va1/f} + S_{Vath}$, and the detector noise $S_{Idet}$.

The resolution of the channel, defined as the minimum detectable variation of the measure and, is expressed in terms of the Equivalent Noise Charge (ENC). The optimal resolution is found for the minimum ENC. The noise matching criterion [9] is applied by setting the proper dimensions of the input transistor of the amplifier in relation to detector and parasitic capacitances that minimizes the ENC. At optimal conditions the dimensions of the input transistor of the preamplifier are provided by the optimal channel width $Z_{opt}$ and the minimum channel length $L_{min}$ (~2 μm) provided by the technology [4,7]

$$Z_{opt} = \frac{2}{3} \frac{C_{det} + C_p}{C_{ox} L_{min}}$$

Fig. 3. Small-signal circuit and noise sources for noise analysis. $C_{det}$ is the detector capacitance, $C_p$ is the parasitic capacitance due to connections between detector and preamplifier, $C_{inp}$ is the amplifier input capacitance, $C_f$ is the feedback capacitance. $S_{Idet}$ noise power spectral density introduced by the detector, and $S_{Va}$ is the noise power spectral density introduced by the amplifier.
where $C_{ox} \approx 3.5 \times 10^{-10}$ F/cm$^2$ is the oxide capacitance per unit area of the input transistor of the amplifier.

The second criterion consists in the minimization of ENC upon shaping time. The optimum is found by equating the detector–amplifier noise corner and the amplifier $1/f$-thermal noise corner [4] as shown in Fig. 4.

This condition provides an optimal drain current $I_{Dopt}$ for the input transistor of the preamplifier (therefore sets the power consumption)

$$I_{Dopt} = \frac{1.95 \times 10^{-3}(kT)^2}{M(I_{Dopt})} \frac{L_{min}C_{ox}^3q^2I_{det}^2}{\mu_{eff}Z_{opt}^2}$$  \hspace{1cm} (2)

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the electron charge, and $\mu_{eff}$ is the channel effective mobility. $M$ is the $1/f$ empirical noise constant that is considered dependent upon the drain current by $M(I_D) = 2.2 \times 10^{-29} \times I_D^{0.7}$, with $I_D$ in amperes, and $M$ in Cb$^2$/cm$^2$ [8].

The optimal shaping time is calculated from

$$\tau_{opt} = 0.23 \frac{kT}{Z_{opt}^{1/2}L_{min}^{3/2}C_{ox}^{3/2}} \frac{1}{M(I_{Dopt})I_{Dopt}^{1/2}}$$  \hspace{1cm} (3)

corresponding to the amplifier $1/f$-thermal noise corner previously mentioned. The shaping time obtained is $\approx 3$ $\mu$s, which is appropriate for a detector having a relatively high collection time.

4. Summary

Multi-channel X-ray and gamma-ray spectroscopy with good energy resolution (FWHM $\approx 5\%$ for photon energies in the order of 150 keV) is highly required in the area of nuclear medicine imaging systems. To this end, a low noise CMOS readout for CdTe and CdZnTe X- and gamma-ray detector arrays has been designed and implemented in the CMOS 2 $\mu$m low noise analog process provided by the multi-chip program of MOSIS [9]. Although a CMOS 2 $\mu$m process is rather old, for analog applications it is often preferred since it is well characterized and exhibits low noise. The readout includes a CMOS CSP optimized for minimum noise for each detector, and a single multiplexed semi-Gaussian pulse shaper. Due to the multiplexed architecture, only one shaper, one peak detector and one comparator are required in the system, utilizing low power and reducing chip area. The optimized CSP provides low noise and low power. Two chips are used, one containing the CSPs and one containing the semi-Gaussian pulse shaper and MUX. The implementation in two chips prevents the coupling between the CSPs and the switches of the multiplexer.

The system implemented leads to high-accuracy multi-channel spectroscopy. In the first prototype chips 32 channels are used. Due to the low-area and low-power consumption more channels can be included in future designs. The main factor limiting further improvement of resolution is the parasitic capacitance due to the connection between the detector and the CSP. This capacitance will be minimized in future designs (less than 1 pf) using indium bumps for the hybrid packaging of the detectors with the corresponding CSPs.

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References

[9] Metal Oxide Semiconductor Implementation Service (MOSIS) A multi chip project fabrication service run by Advanced Research Projects Agency (ARPA), USA.