A Microsystem for ISFET-Based pH Measurement in CMOS Technology

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SUMMARY

The paper presents a complete microsystem for pH measurement based on ISFET sensors. On-chip integration of ISFET sensors, readout, signal processing and serial communication systems was performed in a standard 1.6µm CMOS fabrication process. System architecture allows compatibility for clinical catheter applications, 4-channel sensibility and digital serial output with 2-LSB accuracy. Integration of various interfaces and sensors on 3X0.9 mm² area makes the design suitable for implantable sensor systems.

Keywords: ISFET, CMOS, microsystem.

Subject category: 9. System architecture, intelligent sensor systems.

INTRODUCTION

Since the fabrication of ISFET sensors in regular CMOS process was introduced, the integration of ISFETs with intelligent electronic structures for obtaining on-chip signal processing and implantability is an issue of numerous researches [1,2].

In this paper an ISFET-based CMOS microsystem for pH measurement is presented. The system architecture presentation is followed by test results and layout implementation. A detailed descriptions of ISFET sensors, readout, signal processing, and communication structures are given together with proposals for future improving and extension.

The integration was performed in 3X0.9 mm² area, in 1.6µm CMOS technology, with 5VP-P supply and 2-LSB accuracy observed in 12-bit serial data output.

ISFET-BASED CMOS MICROSYSTEM

A complete microsystem for pH measurement contains four major stages: (a) four ISFET sensors obtaining pH measurements [3], (b) switching and readout interface for sensor selection and conversion of its parameters fluctuations to analog signal, (c) 12-bit Single Slope Analog-to-Digital Converter with parallel output, (d) Parallel-to-Serial Data Converter for communication with serial port of PC. The architecture of the microsystem is given in Fig. 1a.

A schematic structure of a typical application of implantable system is given in Fig. 1b, where a sensor system applied together with reference electrode into a catheter. Because of the limited internal space (typical diameter of 1mm), the demand for minimal area and number of wires is obvious.

Different fabrication styles were used in 4 n-channel ISFETs: (a) passivation of Al gate by Ti-Pt with wide glass opening, (b) passivation with small opening for fabrication misalignment prevention, (c) etching of Al gate with over-gate contacts for improved adhesion and Pt evaporation, (d) etching with near-gate contacts. Active regions have been fixed to W/L=300/30µm and 450µm distance was obtained from encapsulated metal lines to prevent instability and damage at low-pH operation. The reported sensitivity [2] of n-ISFET is 56.6mV/pH. N-channel devices have low-drift properties, but body-effect elimination has to be preserved. An additional set of 700/30µm p-channel ISFETs was implemented in a separate system in similar fabrication styles.

Switching between the sensors was performed by complementary pass-gates controlled by a modulus-5 counter. After completing a 4-sensor cycle, the interface is switched to a ‘dummy’ sensor represented by a VDD bias (Fig. 7a) to allow pattern recognition.

Two types of readout interfaces were implemented for each ISFET class. N-channel sensors were connected to Gate-Feedback interface [4], where because of body-effect constrains, the resistor was relocated and connected in pull-up configuration (Fig. 3a). This improvement allowed a zero Vbs bias, eliminating the body effect. Both circuits are based on 5VP-P operational amplifier.
ISFETs operation was maintained in saturation region, and by equalizing the currents through the resistor and the sensor, following expressions can be derived for output voltage:

\[ I_d = \frac{V_{in} - RV.}{R} = K(V_{out} - VT)^2 \]  
\[ V_{out} = V_m(pH) + \frac{V_{in} - RV.}{K R} \]  

where \( K \) is a constant depending on the technology parameters, and gate size of ISFET. \( Vos \) is maintained constant in this configuration.

For p-channel ISFETs, Source-Feedback circuit was used to obtain the measuring signal (Fig. 3b). Here the equation for output voltage is:

\[ V_{out} = RV. - \frac{I_d}{K} - V_m(pH) \]  

In this circuit a linear dependence of \( V_{OUT} \) on \( VT \) exists and no amplifier needed (an amplifier can be used as a buffer, but not needed for creating feedback). However, in this case, the replacement of current source to a pull up position cannot solve the problem of body effect because there is no expression, for sensor operating in saturation region, which will describe the relationship between \( VOUT \) and \( VT \). This is why only p-ISFETs were used with this readout circuit.

A 12-bit single-slope ADC [5] was chosen for implementation in the microsystem because of low area, accuracy and relatively low operation frequency, typical for pH measurements in blood or CSF. It is described schematically in Fig. 4.

In this technique input voltage is sampled in order to compare it with a ramp voltage that is generated by charging a capacitor by a constant current. Since the rate of ramp rising is known, and maximal value is related to a maximal digital number in the output of the counter, the ramp voltage can be compared with input voltage accompanied by adjusted clock. When both voltages are equal, the clock stops passing through the AND gate and counting is stopped, saving a digital representation of measured analog voltage in the output.

Input voltages were adjusted before the Sample-and-Hold circuit, to enter the 1.2-3.9V linear operation region of the amplifier. An accuracy of 2mV was observed during simulations (Fig. 7b) in conversion of the amplified voltages, corresponding to 0.03pH resolution in the final measurement. The internal 1MHz clock was created by Schmidt generator to feed the 12-bit counter of ADC. An option of external additional clock input was also implemented to avoid high-frequency noise appearance because of internal interactions.

Fig. 3. Readout circuits: (a) gate-feedback configuration, (b) source-feedback configuration

Fig. 4. Structure of single-slope A/D Converter

The data conversion to serial was performed by 13-bit shift register (Fig. 5). A common clock controls all the DFFs. In addition there is a common control on the switches in the inputs of flip-flops. When switches are in position \( a \), the register is loading the parallel data bits from the ADC. When switches are in position \( b \), a serial shifting is preformed, while each clock pulse causes one bit to exit the system. Load input \( a \) of the first DFF is constantly connected to ‘0’, while shifting input \( b \) before the last DFF is connected to ‘1’. This allows obtaining a simple communication protocol, where each 12-bit data bundle is identified by 0-to-1 transition before the bundle and always ends with a 0 value.

Fig. 6 presents the final layout implementation of the microsystem. The integration was performed in 3X0.9 mm\(^2\) area, in 1.6\(\mu\)m CMOS technology. This area allows clinical implantability and can be used for integration in a standard catheter with internal diameter of 1mm.

All the simulation were performed in Cadence, using SpectreS simulator at 27°C and 1-100Hz switching frequency with 5Vp-p supply. The results of the simulations in each of the stages can be seen in Fig. 7.
CLOCK MODULATION

Modulation of clock signals can be considered for implementation to minimize the number of lines dedicated to clock transmission. It demands an external modulation unit and internal detector and clock distributor (band-pass filters), but allows conduction of multiple clock signals through a single line.

Fig. 8 shows the schematic of clock modulation system. It consists of three basic operational units. In the external unit an adder based on operational amplifier is used to combine three sinusoidal signals of different frequencies. Each signal is related to a clock signal with the same frequency that has to be delivered to the internal unit. Detailed implementation of the adder is given in Fig. 9a. After addition a single modulated signal containing information of all three clock channels is delivered to the internal system.

The second stage of the modulation system is clock detector based on three Band Pass Filter structures. A general configuration of second order Band Pass Filter that was used in implementation of first two BPFs for low and medium frequencies is presented in Fig. 9b. In order to determine the parameters of the BPF circuits (namely, $Rr$, $C$ and $R$), following design algorithm was used:

(a) Assume parameters values
(b) Cut-off frequency $f_r$ calculation:
$$ f_r = \frac{0.1125}{RC} \sqrt{\frac{R}{R_r}} $$
(c) Bandwidth $B$ calculation:
$$ B = \frac{0.1591}{RC} $$
(d) Quality factor $Q_p$ calculation:
$$ Q_p = \frac{f_r}{B} $$

If quality factor $Q_p$ is less than 0.5, calculations should be performed again, using new assumptions.
The design of the third high-frequency BPF is based on a general configuration of Fliege High Pass Filter, as presented in [7]. The third stage contains three buffers based on CMOS inverters in the output of each BPF. The buffers are inserted to perform a conversion of sinusoidal signals to digital signals with logic levels suitable for operating the digital controls of the microsystem.

The clock modulator was designed to deliver three clocks of 1 KHz, 10 KHz and 100 KHz to the microsystem. Fig. 10 presents the simulation waveforms received from modulator and detectors. It can be seen that after a short setup time the system is stabilized and a modulated signal from the adder is converted to three separate signals with the expected frequencies.

In addition to hardware design, special MATLAB software was programmed to obtain the automatic system calibration. Its operation is based on Parameter Estimation Theory [6], where for an expected linear model (like ISFET sensitivity), a regression can be best performed for a data sampled from highest and lowest values of deterministic variable (critical pH levels in our case).

CONCLUSIONS

A fully integrated ISFET-based microsystem was presented, followed by an architecture and layout presentation. Test results showing 0.03pH accuracy were presented. The 3X0.9mm² area allows clinical implantability. Clock modulation system was designed and tested in order to allow delivering of multiple clock signals through a single channel and minimizing the number of wires needed for implementation. Multiple sensory channels, body effect elimination analog-to-digital data conversion and serial data output, provide an architectural platform for further improvements. Maintaining these properties, the system can hopefully be used as a basis for advanced clinical applications.

REFERENCES